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Note : Remove "Table of Content" before including in CP Book

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

15EC751: DSP Algorithms and Architecture

A. COURSE INFORMATION

1. Course Overview

Degree:	BE	Program:	BE
Year / Semester :	4/7	Academic Year:	2019-20
Course Title:	DSP Algorithms and Architecture	Course Code:	15EC751
Credit / L-T-P:	3-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	40	SEE Marks:	80 Marks
CIA Marks:	20	Assignment	1 / Module
Course Plan Author:	AMARESH C	Sign	Dt:
Checked By:	Dr. DEVANANDA S N	Sign	Dt:

2. Course Content

Module	Module Content	Teaching Hours	Module Concepts	Blooms Level
1	**Introduction to Digital Signal Processing:** Introduction, A Digital Signal - Processing System, The Sampling Process,Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **Computational Accuracy in DSP Implementations:** Number Formats for Signals and Coefficients in DSP Systems, Dynamic Range and Precision, Sources of Error in DSP Implementation.	8		L1, L2
2	**Architectures for Programmable Digital Signal – Processing Devices:**Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities,	8		L1, L2, L3

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	Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External Interfacing.			
3	**Programmable Digital Signal Processors:** Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS32OC54XX, Memory Space of TMS32OC54xx Processors, Program Control. Detail Study of TMS320C54X & 54xx Instructions and Programming, On -Chip Peripherals, Interrupts of TMS32OC54XX Processors, Pipeline Operation of TMS32OC54xx Processor.	8		L1, L2, L3
4	**Implementation of Basic DSP Algorithms:** Introduction, The Q - notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **Implementation of FFT Algorithms:** Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit - Reversed Index. Generation & Implementation on the TMS32OC54xx.	8		L1, L2, L3
5	**Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices:** Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I/O Direct Memory Access (DMA). **Interfacing and Applications of DSP Processors:** Introduction, Synchronous Serial Interface, A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver, A Speech Processing System,An Image Processing System.	8		L1, L2, L3

3. Course Material

Module	Details	Available
1	Text books	
	"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson Learning, 2004.	In Dept Library
2	Reference books	
	1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B. W Pearson-Education, PHI, 2002. 2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd, 2010 3. "Architectures for Digital Signal Processing", Peter Pirsch John Weily,	In Library

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	2008	
3	Others (Web, Video, Simulation, Notes etc.)	
		Not Available

4. Course Prerequisites

SNo	Course Code	Course Name	Module / Topic / Description	Sem	Remarks	Blooms Level
1	15EC52	Digital Signal Processing	1. Knowledge on Digital Signal Processing	5		L2
2	15EC52	Digital Signal Processing	2.Knowledge of programming	5		L5

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

B. OBE PARAMETERS

1. Course Outcomes

#	COs	Teach. Hours	Concept	Instr Method	Assessment Method	Blooms' Level
CO1	knowledge and concepts of digital signal processing techniques.	04	Multi point sequences	Lecture	Assignment	L2 Understand
CO2	Analyze errors and minimizing errors in implementation	04	Error detection in implementation	Lecture	Assignment	L2 Understand
CO3	Apply knowledge of DSP computational building blocks to achieve speed in DSP architecture or processor.	08	DSP Architecture	Lecture/ PPT	Assignment	L3 Apply
CO4	Apply knowledge of addressing modes ,Interrupts for TMS320C54xx processor.	04	Addressing Modes	Lecture	Assignment /Class test	L3 Apply
CO5	Apply knowledge of peripherals and pipelining structure for TMS320C54xx processor.	04	DSP Interfacing concepts	Lecture	Assignment	L3 Apply
CO6	Evaluate basic DSP algorithms using DSP processors.	08	DSP Processor algorithms	Lecture/ PPT	Assignment	L5 Evaluate
CO7	Discuss about synchronous serial interface and multichannel buffered	04	DSP device interfacing	Lecture	Assignment	L2 Understand

	serial port (McBSP) of DSP device.					
CO8	Understanding Interfacing and applications of DSP Processors	04	DSP Applications	Lecture	Assignment/class test	L2 Apply
-		**40**	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

2. Course Applications

SNo	Application Area	CO	Level
1	Basics of DSP help in designing the algorithms	CO1	L2
2	During implementation process errors can be analyzed and minimized	CO2	L3
3	Understanding architectures, features, Building blocks, memories	CO3	L2
4	Achieve speed in DSP architecture or processor.	CO4	L2
5	Understanding to get the knowledge of architecture addressing modes	CO5	L2
6	How to implement peripherals and pipelining structure for a processor C54xx	CO6	L3
7	Implementing basic DSP algorithms using DSP processors.	CO7	L3
8	knowledge of implementing DSP algotithms of the DSP processor	CO8	L3
9	Understanding of memory and parallel input outputs	CO9	L2
10	Understand how CODEC ,Speech processing and Image processing done	CO10	L2

Note: Write 1 or 2 applications per CO.

3. Articulation Matrix

(CO – PO MAPPING)

-	Course Outcomes	Program Outcomes												
#	COs	PO 1	PO2	PO 3	PO 4	PO 5	PO6	PO 7	PO 8	PO9	PO 10	PO 11	PO 12	Level
EC01PC.1	Basics of DSP help in designing the algorithms	2	1	1	1	1	1	1	1	1	1	1	1	L2
EC501PC.2	During implementation process errors can be analyzed and minimized	3	2	1	1	1	1	1	1	1	1	1	1	L3
EC501PC.3	Understanding architectures, features, Building blocks, memories	2	1	1	1	1	1	1	1	1	1	1	1	L2
EC501PC.4	Achieve speed in DSP architecture or processor.	3	1	1	1	1	1	1	1	1	1	1	1	L2
EC501PC.5	Understanding to get the knowledge of architecture addressing modes	3	1	1	1	1	1	1	1	1	1	1	1	L2
EC501PC.6	How to implement	2	2	1	1	1	1	1	1	1	1	1	1	L3

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	peripherals and pipelining structure for a processor C54xx													
EC501PC.7	Implementing basic DSP algorithms using DSP processors.	3	2	1	1	1	1	1	1	1	1	1	1	L3
EC501PC.8	knowledge of implementing DSP algotithms of the DSP processor	2	2	1	1	1	1	1	1	1	1	1	1	L3
EC501PC.9	Understanding of memory and parallel input outputs	2	2	1	1	1	1	1	1	1	1	1	1	L3
EC501PC.10	Understand how CODEC ,Speech processing and Image processing done	3	1	1	1	1	1	1	1	1	1	1	1	L2
CS501PC.	Average	**2.5**	**1.5**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	
Note: Mention the mapping strength as 1, 2, or 3														

4. Mapping Justification

Mapping		Justification	Mapping Level
CO	**PO**	**-**	**-**
CO1	PO1	Understanding the basic concepts of DSP includes Sampling,DFT,FFT,LTI systmes	L2
	PO2	Solving and applying concepts of decimation and interpolation	L3
	PO3	No design & development concepts included as the concepts are basics of DSP	
	PO4	Investigation are not included as it basic concept	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Basics are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO2	PO1	Understanding the concepts of computing signals and coefficients	L2
	PO2	Applying the concepts for solving the problems related to range and precision	L3
	PO3	No design & development concepts included as the topics are related to precision	

	PO4	Investigation are not included as it related to standard coefficients	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Basics are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO3	PO1	Understanding of architectures are included includes building blocks ,bus architecture and memories	L2
	PO2	Applying of concepts are not necessary as it includes standard architectures	
	PO3	No design & development concepts included as the topics are related to standard architectures	
	PO4	Investigation are not included as it related to building blocks,memories	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO4	PO1	Understanding the concepts of speed issues, Address generation unit, program execution	L2
	PO2	Applying the concepts are required as required as the concepts are standard to architectures	
	PO3	No design & development concepts included as the topics are related to speed issues	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	

	PO12	Its not a life long learning process	
CO5	PO1	Understanding the concepts of different architecture features, addressing modes	L2
	PO2	Applying the concepts are not required as it is related to addressing modes	
	PO3	No design & development concepts included as the topics are related to addressing modes and data addressing	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO6	PO1	Understanding the addressing modes of architecture	L2
	PO2	Applying the knowledge to work with addressing modes	L3
	PO3	No design & development concepts included as the topics are related to addressing modes and data addressing	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO7	PO1	Understanding the concepts of basic DSP algorithms includes Q notation,FIR,IIR concepts	L2
	PO2	Applying the concepts to write algorithms of IIR and FIR concepts	L3
	PO3	No design & development concepts included as the topics are related to algorithms	
	PO4	Investigation are not included as it related to standard concepts of FIR and IIR	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	

	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO8	PO1	Understanding the concepts of DFT computation,Bit reversed index	L2
	PO2	Applying concepts of calculating Bit reversed index generaion	L3
	PO3	No design & development concepts included as the topics are related to interfacing concepts	
	PO4	Investigation are not included as it related to standard concepts of interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO9	PO1	Understanding the concepts of memory and parallel input outputs of memories	
	PO2	Application are not required as concepts are related to memories and Input and outputs	
	PO3	No design & development concepts included as the topics are related to memories	
	PO4	Investigation are not included as it related to standard concepts of memories and IO	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO10	PO1	Understanding the concepts of SSI,CODEC,Speech processing,Image processing	
	PO2	Applying of knowledge is not required	
	PO3	No design & development concepts included as the topics are	

		related to application of DSP	
	PO4	Investigation are not included as it related to standard concepts of DSP applicaitons	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	

Note: Write justification for each CO-PO mapping.

5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Note: Anything not covered above is included here.

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C. COURSE ASSESSMENT

1. Course Coverage

Module #	Title	Teaching Hours	No. of question in Exam						CO	Levels
			CIA-1	CIA-2	CIA-3	Asg	Extra Asg	SEE		
1	Introduction to Digital Signal Processing Computational Accuracy in DSP Implementations	8	2	-	-	1		2	CO1, CO2	L2
2	Architectures for Programmable Digital Signal - Processing Devices:	8	2	-	-	1		2	CO3	L2,L3
3	Programmable Digital Signal Processors	8	-	2	-	1		2	CO4, CO5	L3
4	Implementation of Basic DSP Algorithms	8	-	2	-	1		2	CO6	L5
5	Interfacing Memory and Parallel I/O Peripherals to Programmable DSP Devices Interfacing and Applications of DSP Processors	8	-	-	4	1		2	CO7, C08	L2
-	**Total**	**40**	**4**	**4**	**4**	**5**				

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam – 1	15	CO1, CO2, CO3, CO4	L2, l3,
CIA Exam – 2	15	CO5, CO6,	L3, L5
CIA Exam – 3	15	CO7, C08	L3
Assignment – 1	05	CO1, CO2, CO3, CO4	L2, l3,
Assignment – 2	05	CO5, CO6,	L3, L5
Assignment – 3	05	CO7, C08	L3
Seminar – 1		CO1, CO2, CO3, CO4	L2, l3,
Seminar – 2		CO5, CO6,	L3, L5
Seminar – 3		CO7, C08	L3

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Other Activities – define – Slip test		CO1 to Co8	L2, L3, L5
Final CIA Marks	**20**	**-**	**-**

Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN – 1

Module – 1

Title:	Introduction to Digital Signal Processing Computational Accuracy in DSP Implementations	Appr Time:	8 Hrs
a	***Course Outcomes***	–	**Blooms**
–	The student should be able to:	–	**Level**
1	Understand Basic concepts of DSP system	CO1	L2
2	Apply knowledge to evaluate errors for Implementation	CO2	L3
b	***Course Schedule***	–	–
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction	C01	L2
2	A Digital Signal Processing System The Sampling Process	C01	L2
3	Discrete Time Sequences	C01	L2
4	Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)	C01	L2
5	Linear Time-Invariant Systems	C01	L2
6	Digital Filters	C01	L2
7	Decimation and Interpolation.	C01	L3
8	Number Formats for Signals and Coefficients in DSP Systems	C01	L2
9	Dynamic Range and Precision	C01	L2
10	Sources of Error in DSP Implementation.	C01	L2
c	**Application Areas**	**CO**	**Level**
1	Basics of DSP help in designing the algorithms	CO1	L2
2	During implementation process errors can be analyzed and minimized	CO2	L3
d	**Review Questions**	–	–
1	Explain with the help of mathematical equations how signed numbers can be multiplied. The sequence x(n) = [3,2,–2,0,7].It is interpolated using interpolation sequence bk=[0.5,1,0.5] and the interpolation factor of 2. Find the interpolated sequence y(m)	CO1	L3
2	An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT X(k) determine the analog and digital frequency spacing between adjacent X(k0 elements. Also, determine analog and digital frequencies corresponding to k=60.	CO1	L3

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3	With a neat diagram explain the scheme of the DSP system.	CO1	L2
4	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail.	CO1	L3
5	Why signal sampling is required? Explain the sampling process.	CO1	L2
6	Define decimation and interpolation process. Explain them using block diagrams and equations. With a neat diagram explain the scheme of a DSP system.	CO1	L5
7	With an example explain the need for the low pass filter in decimation process.	CO1	L5
8	For the FIR filter y(n)=(x(n)+x(n-1)+x(n-2))/3. Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay	CO1	L5
9	List the major architectural features used in DSP system to achieve high speed program execution.	CO1	L2
10	Explain how to simulate the impulse responses of FIR and IIR filters.	CO1	L2
11	Explain the two method of sampling rate conversions used in DSP system, with suitable block diagrams and examples. Draw the corresponding spectrum.	CO1	L2
12	Show the dynamic range of a signal increases by6db for each additional bit used to represent its value	CO2	L3
13	Compute the dynamic range and percentage resolution for a block floating point format with a 4 bit exponent used in a 16 bit fixed point processor	CO2	L3
14	Compute the dynamic range and percentage resolution of a signal that uses a. 16 point floating point format b. 32 bit point floating point format with 24 bits for the mantissa and 8 bits for the exponent	CO2	L3
e	**Experiences**	-	-
1			
2			
3			
4			
5			

Module – 2

Title:	Architectures for Programmable Digital Signal – Processing Devices:	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Apply knowledge of DSP computational building blocks to achieve	CO2	L3

	speed in DSP architecture or processor.		
b	***Course Schedule***	–	–
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction		
2	Basic Architectural Features		
3	DSP Computational Building Blocks		
4	Bus Architecture and Memory		
5	Data Addressing Capabilities		
6	Address Generation Unit		
7	Programmability and Program Execution Speed Issues		
8	Features for External Interfacing.		
c	**Application Areas**	**CO**	**Level**
1	Understand DSP processing	CO2	L2
2	Programming DSP processors	CO2	L5
d	**Review Questions**	–	–
1	Explain implementation of 8- tap FIR filter, (i) pipelined using MAC units and (ii) parallel using two MAC units. Draw block diagrams	CO2	L5
2	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram	CO2	L3
3	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	CO2	L5
4	Draw the schematic diagram of the saturation logic and explain the same.	CO2	L3
5	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	CO2	L2
6	Explain the purpose of program sequencer.	CO2	L2
7	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	CO2	L5
8	Explain guard bits in a MAC unit of DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required?	CO2	L5
9	With a neat block diagram explain ALU of DSP system	CO2	L3
10	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	CO2	L3
11	The 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow	CO2	L5
12	How will you implement an 8X8 multiplier using 4X4 multipliers as	CO2	L5

	the building blocks.		
e	**Experiences**	-	-
1		CO1	L2
2			

E1. CIA EXAM – 1

a. Model Question Paper – 1

Crs Code:	15EC751	Sem:	VII	Marks:	30	Time:	75 minutes
Course:	DSP Algorithms and Architecture						

-	-	**Note: Answer any 3 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail.	7	CO1	L5
	b	For the FIR filter y(n)=(x(n)+x(n-1)+x(n-2))/3. Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay	8	CO1	L5
2	a	Explain the two method of sampling rate conversions used in DSP system, with suitable block diagrams and examples. Draw the corresponding spectrum.	7	CO1	L2
	b	Explain with the help of mathematical equations how signed numbers can be multiplied. The sequence x(n) = [3,2,-2,0,7].It is interpolated using interpolation sequence bk=[0.5,1,0.5] and the interpolation factor of 2. Find the interpolated sequence y(m)	8	CO1	L3
3	a	Compute the dynamic range and percentage resolution of a signal that uses a. 16 point floating point format b. 32 bit point floating point format with 24 bits for the mantissa and 8 bits for the exponent	8	CO2	L3
	b	With a neat block diagram explain ALU of DSP system	7	CO2	L2
4	a	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	8	CO2	L5
	b	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	7	CO2	L3

b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

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SNo	USN	Assignment Description	Marks	CO	Level
1	1KT16EC401	Explain with the help of mathematical equations how signed numbers can be multiplied. The sequence x(n) = [3,2,-2,0,7].It is interpolated using interpolation sequence bk=[0.5,1,0.5] and the interpolation factor of 2. Find the interpolated sequence y(m)		CO1	L3
2	1KT15EC001	An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT X(k) determine the analog and digital frequency spacing between adjacent X(k0 elements. Also, determine analog and digital frequencies corresponding to k=60.	5	CO1	L3
3	1KT15EC003	With a neat diagram explain the scheme of the DSP system.		CO1	L2
4	1KT16EC403	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail.	5	CO1	L3
5	1KT15EC004	Why signal sampling is required? Explain the sampling process.	5	CO1	L2
6	1KT15EC005	Define decimation and interpolation process. Explain them using block diagrams and equations. With a neat diagram explain the scheme of a DSP system.	5	CO1	L5
7	1KT15EC006	With an example explain the need for the low pass filter in decimation process.	5	CO1	L5
8	1KT15EC008	For the FIR filter y(n)=(x(n)+x(n-1)+x(n-2))/3. Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay	5	CO1	L5
9	1KT15EC011	List the major architectural features used in DSP system to achieve high speed program execution.	5	CO1	L2
10	1KT16EC406	Explain how to simulate the impulse responses of FIR and IIR filters.	5	CO1	L2
11	1KT15EC012	Explain the two method of sampling rate conversions used in DSP system, with suitable block diagrams and examples. Draw the corresponding spectrum.	5	CO1	L2
12	1KT15EC013	Show the dynamic range of a signal increases by6db for each additional bit used to represent its value	5	CO2	L3
13	1KT15EC015	Compute the dynamic range and percentage resolution for a block floating point format with a 4 bit exponent used in a 16 bit fixed point processor	5	CO2	L3
14	1KT15EC017	Compute the dynamic range and percentage resolution of a signal that uses	5	CO2	L3

		a. 16 point floating point format b. 32 bit point floating point format with 24 bits for the mantissa and 8 bits for the exponent			
15	1KT15EC019	Explain implementation of 8- tap FIR filter, (i) pipelined using MAC units and (ii) parallel using two MAC units. Draw block diagrams	5	CO2	L5
16	1KT14EC068	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram	5	CO2	L3
17	1KT15EC020	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5	CO2	L5
18	1KT15EC021	Draw the schematic diagram of the saturation logic and explain the same.	5	CO2	L3
19	1KT16EC408	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	5	CO2	L2
20	1KT15EC022	Explain the purpose of program sequencer.	5	CO2	L2
21	1KT15EC023	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	5	CO2	L5
22	1KT15EC024	Explain guard bits in a MAC unit of DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required?	5	CO2	L5
23	1KT15EC025	With a neat block diagram explain ALU of DSP system	5	CO2	L3
24	1KT16EC411	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	5	CO2	L3
25	1KT15EC028	The 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow	5	CO2	L5
26	1KT15EC029	How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks.	5	CO2	L5
27	1KT15EC030	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5	CO1	L3
28	1KT15EC031	Draw the schematic diagram of the saturation logic and explain the same.	5	CO1	L3
29	1KT15EC032	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	5	CO1	L2
30	1KT16EC412	Explain the purpose of program sequencer.	5	CO1	L3

31	1KT15EC036	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	5	CO1	L2
32	1KT15EC037	Explain guard bits in a MAC unit of DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required?	5	CO1	L5
33	1KT15EC038	With a neat block diagram explain ALU of DSP system	5	CO1	L5
34	1KT15EC039	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	5	CO1	L5
35	1KT15EC041	The 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow	5	CO1	L2
36	1KT16EC416	How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks.	5	CO1	L2
37	1KT15EC043	Explain implementation of 8- tap FIR filter, (i) pipelined using MAC units and (ii) parallel using two MAC units. Draw block diagrams	5	CO1	L2
38	1KT15EC044	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram	5	CO2	L3
39	1KT15EC045	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5	CO2	L3
40	1KT16EC419	Draw the schematic diagram of the saturation logic and explain the same.	5	CO2	L3
41	1KT15EC046	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	5	CO2	L5
42	1KT15EC047	Explain the purpose of program sequencer.	5	CO2	L3
43	1KT15EC048	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	5	CO2	L5
44	1KT15EC049	Explain guard bits in a MAC unit of DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required?	5	CO2	L3
45	1KT15EC051	With a neat block diagram explain ALU of DSP system	5	CO2	L2
46	1KT15EC052	Explain circular buffer addressing mode ii) Parallelism iii)	5	CO2	L2

		Guard bits			
47	1KT15EC053	The 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow	5	CO2	L5
48	1KT16EC421	How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks.	5	CO2	L5
49	1KT15EC055	Explain implementation of 8- tap FIR filter, (i) pipelined using MAC units and (ii) parallel using two MAC units. Draw block diagrams	5	CO2	L3
50	1KT15EC056	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram	5	CO2	L3
51	1KT15EC058	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5	CO2	L5
52	1KT15EC061	Draw the schematic diagram of the saturation logic and explain the same.	5	CO2	L5
53	1KT16EC423	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	5		
54	1KT16EC424	Explain the purpose of program sequencer.	5		
55	1KT15EC062	Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	5		
56	1KT16EC426	Explain guard bits in a MAC unit of DSP. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required?	5		
57	1KT15EC067	With a neat block diagram explain ALU of DSP system	5		
58	1KT15EC007	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	5		
59	1KT15EC010	The 256 unsigned numbers, 16 bit each are to be summed up in a processor. How many guard bits are needed to prevent overflow	5		
60	1KT15EC014	How will you implement an 8X8 multiplier using 4X4 multipliers as the building blocks.	5		
61	1KT15EC026	Explain implementation of 8- tap FIR filter, (i) pipelined using MAC units and (ii) parallel using two MAC units. Draw block diagrams	5		
62	1KT15EC054	What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a	5		

		diagram			
63	1KT16EC422	Identify the addressing modes of the operands in each of the following instructions & their operations i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5		
64	1KT15EC059	Draw the schematic diagram of the saturation logic and explain the same.	5		
65	1KT15EC063	Explain how the circular addressing mode and bit reversal addressing mode are implemented in a DSP.	5		
66	1KT15EC064	Explain the purpose of program sequencer.	5		
67		Give the structure of a 4X4 Braun multiplier, Explain its concept. What modification is required to carry out multiplication of signed numbers? Comment on the speed of the multiplier	5		

D2. TEACHING PLAN - 2

Module - 3

Title:	Programmable Digital Signal Processors	Appr Time:	8 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Evaluate time and space complexity and calculate performance	CO5	L2
2	Understand searching and sorting schemes	CO6	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction, Commercial Digital Signal-processing Devices	CO3	L2
2	Data Addressing Modes of TMS32OC54XX	CO3	L3
3	Memory Space of TMS32OC54xx Processors	CO3	L2
4	Program Control.	CO3	L2
5	Detail Study of TMS320C54X & 54xx	CO4	L2
6	Instructions and Programming	CO4	L3
7	On - Chip Peripherals	CO4	L3
8	Interrupts of TMS32OC54XX Processors	CO4	L3
c	**Application Areas**	**CO**	**Level**
1	Programming TMS320C54xx processor using data addressing modes	CO3	L3
2	Understand instructions ,on chip peripherals and Interrupts	CO4	L3
d	**Review Questions**	-	-
1	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	CO3	L2

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2	Write an explanatory note on direct addressing mode of TMS320C54XX processors. Give example.	CO3	L3
3	Describe the operation of the following instructions of TMS320C54XX processors. i) MPY *AR2-,*AR4+0B (ii) MAC *ar5+,#1234h,A (iii) STH A,1,*AR2 iv) SSBX SXM	CO3	L2
4	With a block diagram explain the indirect addressing mode of TMS320C54XX processor using dual data memory operand.	CO3	L3
5	What is the function of an address generation unit explain with the help of block diagram.	CO3	L2
6	Why circular buffers are required in DSP processor? How they are implemented?	CO3	L5
7	Explain the direct addressing mode of the TMS320C54XX processor with the help of a block diagram.	CO3	L2
8	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	CO3	L3
9	Describe any four data addressing modes of TMS320c54xx processor	CO3	L3
10	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.	CO3	L2
11	Explain PMST register.	CO3	L2
12	Explain the functioning of barrel shifter in TMS320C54XX processor	CO3	L2
13	Explain sequential and other types of program control	CO3	L2
15	With an example each, explain immediate, absolute, and direct addressing mode.	CO3	L3
16	Explain the functioning of barrel shifter in TMS320C54XX processor.	CO3	L2
17	Explain sequential and other types of program control	CO3	L2
18	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.	CO3	L5
19	Explain PMST register.	CO3	L2
20	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	CO3	L2
21	Describe Host Port Interface and explain its signals.	CO4	L2
22	writes an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2) with usual notations. Find y (n) for signed 16 bit data samples and 16 bit constants.	CO4	L5
23	Describe the pipelining operation of TMS320C54XX processors.	CO4	L3
24	Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals.	CO4	L2
25	Expalin the differents types ofinterrupts in TMS320C54xx Processors.	CO4	L2
26	Describe the operation of the following instructions of TMS 320c54xx	CO4	L3

	processor, with example Describe the operation of hardware timer with neat diagram		
27	By means of a figure explain the pipeline operation of the following sequence of instruction if the initial values of AR1,AR3,A are 104,101,2 and the values stored in the memory locations 101,102,103,104 are 4,6,8,12. Also provide the values of registers AR3, AR1,T & A.	CO4	L4
28	Describe the operation of the following instructions of TMS320C54XX processors.	CO4	L4
29	Describe the operation of the following instructions of TMS320C54XX processors.	CO4	L4
30	Explain the following assembler directives of TMS320C54XX processors (i) .mmregs (ii) .global (iii) .include 'xx' (iv) .data (v) .end (vi) .bss	CO4	L4
31	Describe Host Port Interface and explain its signals.	CO4	L4
32	writes an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2) with usual notations. Find y (n) for signed 16 bit data samples and 16 bit constants.	CO4	L5
33	Describe the pipelining operation of TMS320C54XX processors.	CO4	L2
34	Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals.	CO4	L3
35	Expalin the differents types ofinterrupts in TMS320C54xx Processors.	CO4	L2
e	**Experiences**	-	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

Module - 4

Title:		Appr Time:	16 Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand the Q notation and Different Filters	CO5	L2
2	Able to implement the 8 point Butterfly diagram	CO6	L5
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**

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1	Introduction, The Q – notation	CO5	L3
2	FIR Filters	CO5	L5
3	IIR Filters	CO5	L5
4	Interpolation and Decimation Filters (one example in each case).	CO5	L5
5	Introduction, An FFT Algorithm for DFT Computation	CO6	L2
6	Overflow and Scaling	CO6	L3
7	Bit – Reversed Index.	CO6	L2
8	Generation & Implementation on the TMS32OC54xx.	CO6	L5
c	**Application Areas**	**CO**	**Level**
1	IIR and FIR Filter designing	CO5	L3
2	Overflow and scaling technique	CO6	L5
d	**Review Questions**	–	–
1	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations? Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	CO5	L1
2	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	CO5	L3
3	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	CO5	L2
4	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	CO5	L4
5	Briefly explain IIR filters	CO5	L2
6	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	CO5	L5
7	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) – 0.3125 as a Q15 number.	CO5	L2
8	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	CO5	L3
9	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	CO5	L4
10	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	CO5	L1
11	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) -0.3125 as a Q15 number.	CO5	L4
12	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	CO5	L3
13	Briefly explain IIR filters.	CO2	L2
14	Describe the importance of Q-notation in DSP algorithm	CO5	L3

	implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?		
15	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	CO5	L2
16	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	CO5	L3
17	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	CO5	L4
18	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	CO5	L4
19	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	CO5	L5
20	Derive the equation to implement a butterfly structure In DITFFT algorithm.	CO6	L2
21	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	CO6	L3
22	Why zero padding is done before computing the DFT?	CO6	L2
23	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	CO6	L3
24	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	CO6	L3
25	Explain a general DITFFT butterfly in place computation structure.	CO6	L2
26	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT.	CO6	L3
27	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation.	CO6	L2
28	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors.	CO6	L5
29	Explain, how scaling prevents overflow conditions in the butterfly computation.	CO6	L2
30	Explain, how scaling prevents overflow conditions in the butterfly computation.	CO6	L2
31	With the help of the implementation structure, explain the FFT	CO6	L3

	algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies.		
32	Derive the equation to implement a butterfly structure In DITFFT algorithm.	CO6	L5
33	How many add/subtract and multiply operations are needed to compute the butterfly structure?	CO6	L5
34	Write the subroutine for bit reversed address generation. Explain the same.	CO6	L3
35	Why zero padding is done before computing the DFT?	CO6	L3
36	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	CO6	L3
37	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	CO6	L3
38	With the help of the implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies	CO6	L3
39	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors	CO6	L2
e	**Experiences**	-	-
1			
2			
3			
4			
5			

E2. CIA EXAM – 2

a. Model Question Paper – 2

Crs Code:	15EC751	Sem:	VII	Marks:	30	Time:	75 minutes
Course:	DSP Algorithms and Architecture						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations? Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	8	CO5	L1

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	b	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	7	CO5	L3
2	a	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	8	CO5	L4
	b	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?	7	CO5	L3
3	a	Explain, how scaling prevents overflow conditions in the butterfly computation.	7	CO6	L2
	b	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	8	CO6	L3
4	a	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	7	CO5	L5
	b	Explain a general DITFFT butterfly in place computation structure.	8	CO6	L2

b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	USN	Assignment Description	Marks	CO	Level
1	1KT16EC401	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations? Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L1
2	1KT15EC001	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
3	1KT15EC003	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.		CO5	L2
4	1KT16EC403	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	CO5	L4
5	1KT15EC004	Briefly explain IIR filters	5	CO5	L2
6	1KT15EC005	Determine the value of each of the following 16- bit numbers represented using the given Q-notations: (i)	5	CO5	L5

		0.3125 as a Q15 number (ii) - 0.3125 as a Q15 number.			
7	1KT15EC006	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:(i) 4400h as a Q10 number (ii) 4400h as a Q7 number	5	CO5	L2
8	1KT15EC008	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
9	1KT15EC011	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L4
10	1KT16EC406	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	5	CO5	L1
11	1KT15EC012	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) -0.3125 as a Q15 number.	5	CO5	L4
12	1KT15EC013	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
13	1KT15EC015	Briefly explain IIR filters.	5	CO5	L2
14	1KT15EC017	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?	5	CO5	L3
15	1KT15EC019	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L2
16	1KT14EC068	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
17	1KT15EC020	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	5	CO5	L4
18	1KT15EC021	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	CO5	L4
19	1KT16EC408	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L5
20	1KT15EC022	Derive the equation to implement a butterfly structure In DITFFT algorithm.	5	CO6	L2
21	1KT15EC023	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	5	CO6	L3
22	1KT15EC024	Why zero padding is done before computing the DFT?	5	CO6	L2

23	1KT15EC025	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L3
24	1KT16EC411	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	5	CO6	L3
25	1KT15EC028	Explain a general DITFFT butterfly in place computation structure.	5	CO6	L2
26	1KT15EC029	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT.	5	CO6	L3
27	1KT15EC030	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation.	5	CO6	L2
28	1KT15EC031	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors.	5	CO6	L5
29	1KT15EC032	Explain, how scaling prevents overflow conditions in the butterfly computation.	5	CO6	L2
30	1KT16EC412	Explain, how scaling prevents overflow conditions in the butterfly computation.	5	CO6	L2
31	1KT15EC036	With the help of the implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies.	5	CO6	L3
32	1KT15EC037	Derive the equation to implement a butterfly structure In DITFFT algorithm.	5	CO6	L5
33	1KT15EC038	How many add/subtract and multiply operations are needed to compute the butterfly structure?	5	CO6	L5
34	1KT15EC039	Write the subroutine for bit reversed address generation. Explain the same.	5	CO6	L3
35	1KT15EC041	Why zero padding is done before computing the DFT?	5	CO6	L3
36	1KT16EC416	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L3
37	1KT15EC043	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	5	CO6	L3
38	1KT15EC044	With the help of the implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS320C54XX processors. Use ¼ as a scale factor for all butterflies	5	CO6	L3

39	1KT15EC045	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors	5	CO6	L2
40	1KT16EC419	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations? Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L1
41	1KT15EC046	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
42	1KT15EC047	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	5	CO5	L2
43	1KT15EC048	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	CO5	L4
44	1KT15EC049	Briefly explain IIR filters	5	CO5	L2
45	1KT15EC051	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	5	CO5	L5
46	1KT15EC052	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) – 0.3125 as a Q15 number.	5	CO5	L2
47	1KT15EC053	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
48	1KT16EC421	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L4
49	1KT15EC055	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	5	CO5	L1
50	1KT15EC056	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) –0.3125 as a Q15 number.	5	CO5	L4
51	1KT15EC058	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
52	1KT15EC061	Briefly explain IIR filters.	5	CO2	L2
53	1KT16EC423	Describe the importance of Q-notation in DSP algorithm	5	CO5	L3

		implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?			
54	1KT16EC424	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L2
55	1KT15EC062	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
56	1KT16EC426	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	5	CO5	L4
57	1KT15EC067	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	CO5	L4
58	1KT15EC007	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L5
59	1KT15EC010	Derive the equation to implement a butterfly structure In DITFFT algorithm.	5	CO6	L2
60	1KT15EC014	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	5	CO6	L3
61	1KT15EC026	Why zero padding is done before computing the DFT?	5	CO6	L2
62	1KT15EC054	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L3
63	1KT16EC422	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	5	CO6	L3
64	1KT15EC059	Explain a general DITFFT butterfly in place computation structure.	5	CO6	L2
65	1KT15EC063	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT.	5	CO6	L3
66	1KT15EC064	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation.	5	CO6	L2
67		What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L5

D3. TEACHING PLAN - 3

Module - 5

Title:	Divide and Conquer	Appr Time:	18Hrs
a	***Course Outcomes***	-	**Blooms**
-	The student should be able to:	-	**Level**
1	Understand memories,Bus interfaces,DMA	CO7	L2
2	Understand DSP Interfacing applications	CO8	L3
b	***Course Schedule***		
Class No	**Module Content Covered**	**CO**	**Level**
1	Introduction, Memory Space Organization	CO7	L2
2	External Bus Interfacing Signals.	CO7	L3
3	Memory Interface, Parallel I/O Interface	CO7	L3
4	Programmed I/O,Interrupts and I/O Direct Memory Access	CO7	L5
5	Introduction, Synchronous Serial Interface	CO8	L2
6	A CODEC Interface Circuit,DSP Based Bio-telemetry Receiver	CO8	L3
7	A Speech Processing System	CO8	L3
8	An Image Processing System.	CO8	L3
c	**Application Areas**	**CO**	**Level**
1	Memory interfacing with DSP processor	CO7	L3
2	Interrupts and Parallel I/O Interrupts	CO8	L4
d	**Review Questions**	-	-
1	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	CO7	L1
2	Describe DMA with respect to TMS320C54XX processors	CO7	L3
3	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	CO7	L2
4	Explain the memory interface block diagram for the TMS 320 C54xx processor.	CO7	L3
5	Draw the I/O interface timing diagram for read - write read sequence of operation.	CO8	L2
6	What are interrupts? How interrupts are handled by C54xx DSP Processors.	CO8	L4
7	Explain the memory interface block diagram for the TMS 320 C54xx processor.	CO8	L3
8	Draw the I/O interface timing diagram for read - write read sequence of operation.	CO8	L3
9	What are interrupts? How interrupts are handled by C54xx DSP Processors.	CO8	L3

10	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	CO8	L5
11	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	CO8	L4
12	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	CO8	L3
13	Describe DMA with respect to TMS320C54XX processors.	CO8	L2
14	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	CO8	L3
15	Explain the memory interface block diagram for the TMS 320 C54xx processor.	CO8	L3
16	Draw the I/O interface timing diagram for read – write read sequence of operation	CO8	L5
17	What are interrupts? How interrupts are handled by C54xx DSP Processors.	CO8	L3
18	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	CO8	L3
19	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	CO8	L4
20	Write a pseudo algorithm heart rate(HR), using the digital signal processor.	CO8	L3
21	Explain briefly the building blocks of a PCM3002 CODEC device. What do you understand by a DSP based biotelemetry receiver?	CO8	L3
22	With the help of block diagram explain JPEG algorithm.	CO8	L3
23	Explain with the neat diagram the operation of pitch detector.	CO8	L3
24	Explain with a neat diagram, the synchronous serial interface between the C54xx and a CODEC device. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals.	CO8	L3
25	Explain with a neat block diagram the operation, the operation of the pitch detector.	CO8	L3
26	Explain PCM3002 CODEC, with the help of neat block diagram.	CO8	L3
27	Explain DSP based biotelemetry receiver system, with the help of a block schematic diagram.	CO8	L3
28	Explain the memory interface block diagram for the TMS 320 C54xx processor.	CO8	L3
29	Draw the I/O interface timing diagram for read – write read sequence of operation	CO8	L3
30	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	CO8	L3
e	**Experiences**	-	-
1			
2			

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E3. CIA EXAM – 3

a. Model Question Paper – 3

Crs Code:	15EC751	Sem:	VII	Marks:	30	Time:	75 minutes
Course:	DSP Algorithms and Architecture						

-	-	**Note: Answer any 2 questions, each carry equal marks.**	**Marks**	**CO**	**Level**
1	a	Explain the memory interface block diagram for the TMS 320 C54xx processor.	7	CO7	L3
	b	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	8	CO7	L2
2	a	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	7	CO7	L1
	b	Describe DMA with respect to TMS320C54XX processors		CO7	L3
3	a	Draw the I/O interface timing diagram for read – write read sequence of operation	8	CO8	L5
	b	Describe DMA with respect to TMS320C54XX processors.	7	CO8	L2
4	a	Explain PCM3002 CODEC, with the help of neat block diagram.	8	CO8	L3
	b	Explain DSP based biotelemetry receiver system, with the help of a block schematic diagram.	7	CO8	L3

b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	VII	Marks:	5	Time:	90 – 120 minutes
Course:	Design and Analysis of Algorithms						
Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.							

SNo	**USN**	**Assignment Description**	**Marks**	**CO**	**Level**
1	1KT16EC401	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO7	L1
2	1KT15EC001	Describe DMA with respect to TMS320C54XX processors	5	CO7	L3
3	1KT15EC003	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	5	CO7	L2
4	1KT16EC403	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO7	L3
5	1KT15EC004	Draw the I/O interface timing diagram for read – write read sequence of operation.	5	CO8	L2

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6	1KT15EC005	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L4
7	1KT15EC006	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
8	1KT15EC008	Draw the I/O interface timing diagram for read – write read sequence of operation.	5	CO8	L3
9	1KT15EC011	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L3
10	1KT16EC406	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L5
11	1KT15EC012	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L4
12	1KT15EC013	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO8	L3
13	1KT15EC015	Describe DMA with respect to TMS320C54XX processors.	5	CO8	L2
14	1KT15EC017	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	5	CO8	L3
15	1KT15EC019	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
16	1KT14EC068	Draw the I/O interface timing diagram for read – write read sequence of operation	5	CO8	L5
17	1KT15EC020	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L3
18	1KT15EC021	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	5	CO8	L3
19	1KT16EC408	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	5	CO8	L4
20	1KT15EC022	Write a pseudo algorithm heart rate(HR), using the digital signal processor.	5	CO8	L3
21	1KT15EC023	Explain briefly the building blocks of a PCM3002 CODEC device. What do you understand by a DSP based biotelemetry receiver?	5	CO8	L3
22	1KT15EC024	With the help of block diagram explain JPEG algorithm.	5	CO8	L3
23	1KT15EC025	Explain with the neat diagram the operation of pitch detector.	5	CO8	L3
24	1KT16EC411	Explain with a neat diagram, the synchronous serial interface between the C54xx and a CODEC device. Explain the operation of pulse position modulation (PPM) to	5	CO8	L3

		encode two biomedical signals.			
25	1KT15EC028	Explain with a neat block diagram the operation, the operation of the pitch detector.	5	CO8	L3
26	1KT15EC029	Explain PCM3002 CODEC, with the help of neat block diagram.	5	CO8	L3
27	1KT15EC030	Explain DSP based biotelemetry receiver system, with the help of a block schematic diagram.	5	CO8	L3
28	1KT15EC031	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
29	1KT15EC032	Draw the I/O interface timing diagram for read – write read sequence of operation	5	CO8	L3
30	1KT16EC412	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	5	CO8	L3
31	1KT15EC036	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO7	L1
32	1KT15EC037	Describe DMA with respect to TMS320C54XX processors	5	CO7	L3
33	1KT15EC038	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	5	CO7	L2
34	1KT15EC039	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO7	L3
35	1KT15EC041	Draw the I/O interface timing diagram for read – write read sequence of operation.	5	CO8	L2
36	1KT16EC416	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L4
37	1KT15EC043	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
38	1KT15EC044	Draw the I/O interface timing diagram for read – write read sequence of operation.	5	CO8	L3
39	1KT15EC045	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L3
40	1KT16EC419	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L5
41	1KT15EC046	Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L4
42	1KT15EC047	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO8	L3
43	1KT15EC048	Describe DMA with respect to TMS320C54XX processors.	5	CO8	L2
44	1KT15EC049	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of	5	CO8	L3

		each signal involved.			
45	1KT15EC051	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
46	1KT15EC052	Draw the I/O interface timing diagram for read – write read sequence of operation	5	CO8	L5
47	1KT15EC053	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L3
48	1KT16EC421	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	5	CO8	L3
49	1KT15EC055	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	5	CO8	L4
50	1KT15EC056	Write a pseudo algorithm heart rate(HR), using the digital signal processor.	5	CO8	L3
51	1KT15EC058	Explain briefly the building blocks of a PCM3002 CODEC device. What do you understand by a DSP based biotelemetry receiver?	5	CO8	L3
52	1KT15EC061	With the help of block diagram explain JPEG algorithm.	5	CO8	L3
53	1KT16EC423	Explain with the neat diagram the operation of pitch detector.	5	CO8	L3
54	1KT16EC424	Explain with a neat diagram, the synchronous serial interface between the C54xx and a CODEC device. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals.	5	CO8	L3
55	1KT15EC062	Explain with a neat block diagram the operation, the operation of the pitch detector.	5	CO8	L3
56	1KT16EC426	Explain PCM3002 CODEC, with the help of neat block diagram.	5	CO8	L3
57	1KT15EC067	Explain DSP based biotelemetry receiver system, with the help of a block schematic diagram.	5	CO8	L3
58	1KT15EC007	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
59	1KT15EC010	Draw the I/O interface timing diagram for read – write read sequence of operation	5	CO8	L3
60	1KT15EC014	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	5	CO8	L3
61	1KT15EC026	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO7	L1
62	1KT15EC054	Describe DMA with respect to TMS320C54XX processors	5	CO7	L3
63	1KT16EC422	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	5	CO7	L2

64	1KT15EC059	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO7	L3
65	1KT15EC063	Draw the I/O interface timing diagram for read – write read sequence of operation.	5	CO8	L2
66	1KT15EC064	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L4
67		Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3

F. EXAM PREPARATION

1. University Model Question Paper

Course:	DSP Algorithms and Architecure					Month / Year	May /2018	
Crs Code:	CS501PC	Sem:	I	Marks:	100	Time:	180 minutes	
–	**Note**	Answer all FIVE full questions. All questions carry equal marks.				**Marks**	**CO**	**Level**
1	a	With a neat diagram explain the scheme of the DSP system. Draw the wave forms				08	CO1	L3
	b	Let x[n] = [3, 2, –2, 0, 7]. It is interpolated using an interpolation filter bk = [0.5, 1, 0.5] with interpolation factor 2. Determine the interpolated sequence.				07	CO1	L3
		OR						
–	a	Explain number formats for signals and co efficients in DSP systems				07	CO2	L2
	b	Explain dynamic range and Precession				08	CO2	L2
2	a	How does the barrel shifter in a DSP works? Explain with an example.				07	CO3	L2
	b	Explain : i) circular addressing mode ii) parallelism iii) Guard bits				09	CO3	L3
		OR						
–	a	Explain the bit reversed addressing mode for a 16 point FFT with a neat diagram and step by step generation of binary code.				08	CO3	L2
	b	With a neat block diagram, explain the working of MAC unit.				07	CO3	L3
3	a	Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP				06	CO4	L3
	b	Explain any five addressing modes of TMS320C54XX with one example each.				10	CO4	L5
–	a	Identify the addressing modes of the source operand in each of the following instructions: (i) ADD, *AR2+0B, A (ii) ADD *AR2+, A (iii) ADD *AR2+%, A (iv) 3a DD #23h, A				10	CO5	L5
	b	Explain the following assembler directives of TMS320C54XX processors. i) · mmregs ii) · global iii) · include'xx' iv) · data v) · end vi) · bss				06	CO5	L5

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4	a	Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a QO number ii) 4400h as a Q7 number·3125 as a Q15 number iv) 3125 as a Q15 number.	06	CO6	L5
	b	Write an ALP for the FIR filter with 200 input samples using 16 length circular buffers for the TMS320 DSP	10	CO6	L5
		OR			
-	a	Write a pseudo code to determine 8 point DFT using DIT FFT algorithm invoking butterfly subroutine in a nested loop for each stage	08	CO6	L3
	b	Write an ALP to multiply two Q15 numbers to produce a Q15 result for the TMS320 DSP	07	CO5	L3
5	a	Explain the working of DMA with respect to the TMS320 DSP processor.	08	CO7	L2
	b	Explain the working of interrupts in TMS320 DSP	07	CO7	L2
		OR			
	a	Explain the biotelemetry receiver system with the help of a block diagram.	07	CO8	L3
	b	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	08	CO8	L3

2. SEE Important Questions

Course:	Design and Analysis of Algorithms					Month / Year	May /2018
Crs Code:	CS501PC	Sem:	3	Marks:	100	Time:	180 minutes

	Note	Answer all FIVE full questions. All questions carry equal marks.	-	-	
Module	Qno.	Important Question	**Marks**	**CO**	**Year**
1	1	With a neat diagram explain the scheme of the DSP system.	06	CO1	2018
	2	Mention the difference between FIR and IIR filters. Find the magnitude and phase response of an FIR filter represented by the difference equation, y(n) = 0.5x(n)— 0.5x(n —1)	06	CO1	2018
	3	Let x[n] = [3, 2, -2, 0, 7]. It is interpolated using an interpolation filter bk = [0.5, 1, 0.5] with interpolation factor 2. Determine the interpolated sequence.	06	CO1	2017
	4	An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT x(k), determine analog and digital frequency spacing between adjacent x(k) elements. Also,	06	CO1	2017

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		determine analog and digital frequencies corresponding to K=64			
	5	Explain number formats for signals and co efficients in DSP systems	08	C02	New
2	1	How does the barrel shifter in a DSP works? Explain with an example.	06	CO3	2018
	2	Explain : i) circular addressing mode ii) parallelism iii) Guard bits	09	CO3	2017
	3	With a neat block diagram, explain the working of MAC unit	08	CO3	2017
	4	Explain the bit reversed addressing mode for a 16 point FFT with a neat diagram and step by step generation of binary code.	08	CO3	2018
	5	With a neat block diagram, explain the working of MAC unit.	06	CO3	2015
3	1	Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP	06	CO4	2018
	2	Explain any five addressing modes of TMS320C54XX with one example each.	10	CO4	2017
	3	Explain the addressing modes of TMS320C54XX processor. Give examples.	10	CO4	2018
	4	Identify the addressing modes of the source operand in each of the following instructions: (i) ADD, *AR2+0B, A (ii) ADD *AR2+, A (iii) ADD *AR2+%, A (iv) 3a DD #23h, A	10	CO5	2018
	5	Explain the following assembler directives of TMS320C54XX processors. i) · mmregs ii) · global iii) · include'xx' iv) · data v) · end vi) · bss	06	CO5	2016
4	1	Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a QO number ii) 4400h as a Q7 number·3125 as a Q15 number iv) 3125 as a Q15 number.	06	CO6	2017
	2	Write an ALP for the FIR filter with 200 input samples using 16 length circular buffers for the TMS320 DSP	10	CO6	2018
	3	explain scaling operation in DSP processor and derive the expression for optimal scaling factor for DIT FFT butterfly algorithm.	08	CO6	2018
	4	Write a pseudo code to determine 8 point DFT using DIT FFT algorithm invoking butterfly subroutine in a nested loop for each stage	12	CO6	2017
	5	Write an ALP to multiply two Q15 numbers to produce a Q15 result for the TMS320 DSP	06	CO5	2017
5	1	Explain the working of DMA with respect to the TMS320 DSP processor.	08	CO7	2018
	2	Explain the working of interrupts in TMS320 DSP	06	CO7	2018
	3	With a neat schematic diagram, design a data memory system with address range 000800h — 00OFFFH for a C5416 processor. Use	08	CO7	2017

		2Kx8 SRAM memory chips.			
	4	Explain the biotelemetry receiver system with the help of a block diagram.	06	CO8	2018
	5	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	08	CO8	2017