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Note : Remove "Table of Content" before including in CP Book

Each Course Plan shall be printed and made into a book with cover page

Blooms Level in all sections match with A.2, only if you plan to teach / learn at higher levels

# 15EC751: DSP Algorithms and Architecture

### A. COURSE INFORMATION

#### 1. Course Overview

Degree:	BE	Program:	BE
Year / Semester :	4/7	Academic Year:	2019-20
Course Title:	DSP Algorithms and Architecture	Course Code:	15EC751
Credit / L-T-P:	3-0-0	SEE Duration:	180 Minutes
Total Contact Hours:	40	SEE Marks:	80 Marks
CIA Marks:	20	Assignment	1 / Module
Course Plan Author:	AMARESH C	Sign	Dt:
Checked By:	Dr. DEVANANDA S N	Sign	Dt:

### 2. Course Content

Mod	Module Content	Teaching	Module	Blooms
ule		Hours	Concepts	Level
1	Introduction to Digital Signal Processing: Introduction,	8		L1, L2
	A Digital Signal - Processing System, The Sampling			
	Process,Discrete Time Sequences, Discrete Fourier			
	Transform (DFT) and Fast Fourier Transform (FFT), Linear			
	Time-Invariant Systems, Digital Filters, Decimation and			
	Interpolation.			
	<b>Computational Accuracy in DSP Implementations:</b>			
	Number Formats for Signals and Coefficients in DSP			
	Systems, Dynamic			
	Range and Precision, Sources of Error in DSP			
	Implementation.			
2	Architectures for Programmable Digital Signal –	8		L1, L2,
	Processing Devices:Introduction, Basic Architectural			L3
	Features, DSP Computational Building Blocks, Bus			
	Architecture and Memory, Data Addressing Capabilities,			

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	Address Generation Unit, Programmability and Program		
	Execution, Speed Issues, Features for External Interfacing.		
3	Programmable Digital Signal Processors:	8	L1, L2,
	Introduction, Commercial Digital Signal-processing Devices,		L3
	Data		
	Addressing Modes of TMS32OC54XX, Memory Space of		
	TMS32OC54xx Processors, Program Control. Detail Study of		
	TMS320C54X & 54xx Instructions and Programming, On -		
	Chip Peripherals, Interrupts of TMS32OC54XX Processors,		
	Pipeline Operation of TMS32OC54xx Processor.		
4	Implementation of Basic DSP Algorithms:	8	L1, L2,
	Introduction, The Q - notation, FIR Filters, IIR Filters,		L3
	Interpolation and Decimation Filters (one example in each		
	case).		
	Implementation of FFT Algorithms:		
	Introduction, An FFT Algorithm for DFT Computation,		
	Overflow and Scaling, Bit - Reversed Index. Generation &		
	Implementation on the TMS32OC54xx.		
5	Interfacing Memory and Parallel I/O Peripherals to	8	L1, L2,
	Programmable DSP Devices:		L3
	Introduction, Memory Space Organization, External Bus		
	Interfacing Signals. Memory Interface, Parallel I/O Interface,		
	Programmed I/O, Interrupts and I/O Direct Memory Access		
	(DMA).		
	Interfacing and Applications of DSP Processors:		
	Introduction, Synchronous Serial Interface, A CODEC		
	Interface Circuit, DSP Based Bio-telemetry Receiver, A		
	Speech Processing System, An Image Processing System.		

### 3. Course Material

Mod	Details	Available
ule		
1	Text books	
	"Digital Signal Processing", Avatar Singh and S. Srinivasan, Thomson	In Dept Library
	Learning, 2004.	
2	Reference books	
	1. "Digital Signal Processing: A practical approach", Ifeachor E. C., Jervis B.	In Library
	W	
	Pearson-Education, PHI, 2002.	
	2. "Digital Signal Processors", B Venkataramani and M Bhaskar, TMH, 2nd,	
	2010	
	3. "Architectures for Digital Signal Processing", Peter Pirsch John Weily,	

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	2008				
3	3 Others (Web, Video, Simulation, Notes etc.)				
				Not Available	

### 4. Course Prerequisites

SNo	Course	Course Name	Module / Topic / Description	Sem	Remarks	Blooms
	Code					Level
1	15EC52	Digital Signal	1. Knowledge on Digital Signal	5		L2
		Processing	Processing			
2	15EC52	Digital Signal	2.Knowledge of programming	5		L5
		Processing				

Note: If prerequisites are not taught earlier, GAP in curriculum needs to be addressed. Include in Remarks and implement in B.5.

#### **B. OBE PARAMETERS**

#### 1. Course Outcomes

#	COs	Teach.	Concept	Instr	Assessmen	Blooms'
		Hours		Method	t Method	Level
CO1	knowledge and concepts of digital	04	Multi point	Lecture	Assignmen	L2
	signal processing techniques.		sequences		t	Understand
CO2	Analyze errors and minimizing	04	Error	Lecture	Assignmen	L2
	errors in implementation		detection in		t	Understand
			implementa			
			tion			
CO3	Apply knowledge of DSP	08	DSP	Lecture/	Assignmen	L3
	computational building blocks to		Architectur	PPT	t	Apply
	achieve speed in DSP architecture or		е			
	processor.					
CO4	Apply knowledge of addressing	04	Addressing	Lecture	Assignmen	L3
	modes ,Interrupts for TMS320C54xx		Modes		t /Class	Apply
	processor.				test	
CO5	Apply knowledge of peripherals and	04	DSP	Lecture	Assignmen	L3
	pipelining structure for		Interfacing		t	Apply
	TMS320C54xx processor.		concepts			
CO6	Evaluate basic DSP algorithms using	08	DSP	Lecture/	Assignmen	L5
	DSP processors.		Processor	PPT	t	Evaluate
			algorithms			
C07	Discuss about synchronous serial	04	DSP device	Lecture	Assignmen	L2
	interface and multichannel buffered		interfacing		t	Understand

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	serial port (McBSP) of DSP devic	ce.					
CO8	Understanding Interfacing	and	04	DSP	Lecture	Assignmen	L2
	applications of DSP Processors			Application		t/class test	Apply
				S			
-			40	-	-	-	-

Note: Identify a max of 2 Concepts per Module. Write 1 CO per concept.

### 2. Course Applications

SNo	Application Area	CO	Level
1	Basics of DSP help in designing the algorithms	CO1	L2
2	During implementation process errors can be analyzed and minimized	CO2	L3
3	Understanding architectures, features, Building blocks, memories	CO3	L2
4	Achieve speed in DSP architecture or processor.	CO4	L2
5	Understanding to get the knowledge of architecture addressing modes	CO5	L2
6	How to implement peripherals and pipelining structure for a processor C54xx	CO6	L3
7	Implementing basic DSP algorithms using DSP processors.	C07	L3
8	knowledge of implementing DSP algotithms of the DSP processor	CO8	L3
9	Understanding of memory and parallel input outputs	CO9	L2
10	Understand how CODEC ,Speech processing and Image processing done	CO10	L2
N	Write 1 or 2 applications per CO		

Note: Write 1 or 2 applications per CO.

#### 3. Articulation Matrix

#### (CO – PO MAPPING)

_	Course Outcomes	Program Outcomes												
#	COs PC			PO	PO	PO	PO6	PO	PO	PO9	PO	PO	PO	Level
		1		3	4	5		7	8		10	11	12	
EC01PC.1	Basics of DSP help in	2	1	1	1	1	1	1	1	1	1	1	1	L2
	designing the algorithms													
EC501PC.2	During implementation	3	2	1	1	1	1	1	1	1	1	1	1	L3
	process errors can be													
	analyzed and minimized													
EC501PC.3	Understanding architectures,	2	1	1	1	1	1	1	1	1	1	1	1	L2
	features, Building blocks,													
	memories													
EC501PC.4	Achieve speed in DSP	3	1	1	1	1	1	1	1	1	1	1	1	L2
	architecture or processor.													
EC501PC.5	Understanding to get the	3	1	1	1	1	1	1	1	1	1	1	1	L2
	knowledge of architecture													
	addressing modes													
EC501PC.6	How to implement	2	2	1	1	1	1	1	1	1	1	1	1	L3

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	peripherals	and pipelining	

Note: Menti	ion the mapping strength as	s 1,	2, o	r 3										
CS501PC.	Average	2.5	1.5	1	1	1	1	1	1	1	1	1	1	
	Image processing done													
	,Speech processing and													
EC501PC.10	Understand how CODEC	3	1	1	1	1	1	1	1	1	1	1	1	L2
	and parallel input outputs													
EC501PC.9	Understanding of memory	2	2	1	1	1	1	1	1	1	1	1	1	L3
	processor													
	DSP algotithms of the DSP													
EC501PC.8	knowledge of implementing	2	2	1	1	1	1	1	1	1	1	1	1	L3
	processors.													
	algorithms using DSP													
EC501PC.7	Implementing basic DSP	3	2	1	1	1	1	1	1	1	1	1	1	L3
	C54xx													
	structure for a processor													
	peripherals and pipelining													

# 4. Mapping Justification

Мар	oping	Justification	Mapping Level				
CO	PO	-	-				
CO1	PO1	Understanding the basic concepts of DSP includes Sampling,DFT,FFT,LTI systmes	L2				
	PO2	Solving and applying concepts of decimation and interpolation	L3				
	PO3	No design & development concepts included as the concepts are basics of DSP					
	PO4	Investigation are not included as it basic concept					
	PO5	Tools are not required for these topics					
	PO6	Its not related to society usage					
	PO7	Basics are not used for environment and sustainability					
	PO8	No ethics are included in this topic					
	PO9	No team work is required to know basics					
	PO10	Communication and any documentation not required					
	PO11	Project management and finance management are not needed					
	PO12	Its not a life long learning process					
CO2	PO1	Understanding the concepts of computing signals and coefficients	L2				
	PO2	Applying the concepts for solving the problems related to range and precision	L3				
	PO3	No design & development concepts included as the topics are related to precision					

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	PO4	Investigation are not included as it related to sta	andard
		coefficients	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Basics are not used for environment and sustainability	

	PO7	Basics are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO3	PO1	Understanding of architectures are included includes building L2 blocks ,bus architecture and memories	2
	PO2	Applying of concepts are not necessary as it includes standard architectures	
	PO3	No design & development concepts included as the topics are related to standard architectures	
	PO4	Investigation are not included as it related to building blocks,memories	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO4	PO1	Understanding the concepts of speed issues, AddressL2 generation unit, program execution	
	PO2	Applying the concepts are required as required as the concepts are standard to architectures	
	PO3	No design & development concepts included as the topics are related to speed issues	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	

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,	cAAS. All rights res PO12	Its not a life long learning process	
CO5	PO1	Understanding the concepts of different architecture features, addressing modes	L2
	PO2	Applying the concepts are not required as it is related to addressing modes	
	PO3	No design & development concepts included as the topics are related to addressing modes and data addressing	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
CO6	PO1	Understanding the addressing modes of architecture	L2
	PO2	Applying the knowledge to work with addressing modes	L3
	PO3	No design & development concepts included as the topics are	
		related to addressing modes and data addressing	
	PO4	Investigation are not included as it related to speed issues and interfacing	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
C07	PO1	Understanding the concepts of basic DSP algorithms includes Q notation,FIR,IIR concepts	L2
	PO2	Applying the concepts to write algorithms of IIR and FIR concepts	L3
	PO3	No design & development concepts included as the topics are related to algorithms	
	PO4	Investigation are not included as it related to standard concepts of FIR and IIR	<u> </u>
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	

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P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C08       P01       Understanding the concepts of DFT computation,Bit reversedL2 index         P02       Applying concepts of calculating Bit reversed index generaion       L3         P03       No design & development concepts included as the topics are related to interfacing concepts       Index         P04       Investigation are not included as it related to standard concepts of interfacing       P05       Tools are not required for these topics         P06       Its not related to society usage       P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic       P08       No team work is required to know basics         P010       Communication and any documentation not required       P011       Project management and finance management are not needed         P011       Project management and guadatic process       P010       Communication and any documentation not required         P0111       Project management anot re	Copyright ©2017. cA	AAS. All rights reser	rved.	-
P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C08       P01       Understanding the concepts of DFT computation,Bit reversedL2 index         P02       Applying concepts of calculating Bit reversed index generation       L3         P03       No design & development concepts included as the topics are related to interfacing concepts       P04         P04       Investigation are not included as it related to standard concepts of interfacing       P05         P05       Tools are not required for these topics       P06         P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P0112       Project management and finance management are not needed         P012       Its not a life long learning process         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not required as concepts are related to memories and Input and outputs         P03       No d				
P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C08       P01       Understanding the concepts of DFT computation,Bit reversedL2 index         P02       Applying concepts of calculating Bit reversed index generation       L3         P03       No design & development concepts included as the topics are related to interfacing concepts       Investigation are not included as it related to standard concepts of interfacing         P04       Investigation are not included as it related to standard concepts         P05       Tools are not required for these topics         P06       Its not related to society usage         P07       Architectures are not used for environment and sustainability         P08       No etains or is required to know basics         P010       Communication and any documentation not required         P0112       Its not a life long learning process         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not included as it related to standard concepts of memories and lnput and outputs         P03       No design & development concepts included as the topics are related to memories         P04       Investigation are not included as it related		PO8	No ethics are included in this topic	
P011       Project management and finance management are not needed         P012       Its not a life long learning process         C08       P01       Understanding the concepts of DFT computation,Bit reversedL2 index         P02       Applying concepts of calculating Bit reversed index generation       L3         P03       No design & development concepts included as the topics are related to interfacing concepts       L3         P04       Investigation are not included as it related to standard concepts of interfacing       P05         P05       Tools are not required for these topics       P06         P06       Its not related to society usage       P07         P07       Architectures are not used for environment and sustainability       P08         P09       No team work is required to know basics       P010         P010       Communication and any documentation not required       P011         P011       Project management and finance management are not needed       P012         P012       Its not a life long learning process       C09         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not included as it related to standard concepts of memories and lnput and outputs         P03       No design & development concepts included as the topics are related to memorie		PO9	No team work is required to know basics	
P012       Its not a life long learning process         C08       P01       Understanding the concepts of DFT computation,Bit reversedL2 index         P02       Applying concepts of calculating Bit reversed index generation       L3         P03       No design & development concepts included as the topics are related to interfacing concepts       Investigation are not included as it related to standard concepts of interfacing         P05       Tools are not required for these topics       P06         P06       Its not related to society usage       P07         P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not required as concepts are related to memories and Input and outputs         P03       No design & development concepts included as the topics are related to memories         P04       Investigation are not included as it related to standard concepts of memories and IO         P05       Tools are no		PO10	Communication and any documentation not required	
CO8       P01       Understanding the concepts of DFT computation,Bit reversed L2 index         PO2       Applying concepts of calculating Bit reversed index generation       L3         PO3       No design & development concepts included as the topics are related to interfacing concepts       L3         PO4       Investigation are not included as it related to standard concepts of interfacing       P05         PO5       Tools are not required for these topics       P06         PO7       Architectures are not used for environment and sustainability         PO8       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         CO9       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not required as it related to standard concepts of memories and lnput and outputs         P03       No design & development concepts included as the topics are related to memories and lo         P04       Investigation are not included as it related to standard concepts of memories and lO         P05       Tools are not required for these topics         P06       Its not related to so		PO11	Project management and finance management are not needed	
index       Index         PO2       Applying concepts of calculating Bit reversed index generation       L3         PO3       No design & development concepts included as the topics are related to interfacing concepts       Investigation are not included as it related to standard concepts of interfacing         PO5       Tools are not required for these topics       Investigation are not society usage         PO5       Tools are not required for these topics       Investigation are not used for environment and sustainability         PO6       Its not related to society usage       Investigation are included in this topic         PO9       No team work is required to know basics       Investigation and any documentation not required         PO10       Communication and any documentation not required       PO11         PO11       Project management and finance management are not needed       PO12         PO12       Its not a life long learning process       Investigation are not required as concepts are related to memories and lnput and outputs         PO3       No design & development concepts included as the topics are related to memories and Input and outputs         PO3       No design & development concepts included as the topics are related to memories and Io         PO3       No design & development concepts included as the topics are related to memories and Io         PO4       Investigation are not included as it related to standard concep		PO12	Its not a life long learning process	
P03       No design & development concepts included as the topics are related to interfacing concepts         P04       Investigation are not included as it related to standard concepts of interfacing         P05       Tools are not required for these topics         P06       Its not related to society usage         P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P03       No design & development concepts included as the topics are related to memories and lnput and outputs         P03       No design & development concepts included as the topics are related to memories and IO         P04       Investigation are not included as it related to standard concepts of memories and IO         P05       Tools are not required for these topics         P06       Its not related to society usage         P06       Its not related to society usage         P07       Architectures are not used for environment and sustainability	CO8	PO1		L2
related to interfacing concepts       related to standard concepts of interfacing         PO4       Investigation are not included as it related to standard concepts of interfacing         PO5       Tools are not required for these topics         PO6       Its not related to society usage         PO7       Architectures are not used for environment and sustainability         PO8       No ethics are included in this topic         PO9       No team work is required to know basics         PO10       Communication and any documentation not required         PO11       Project management and finance management are not needed         PO12       Its not a life long learning process         CO9       PO1       Understanding the concepts of memory and parallel input outputs of memories         PO2       Application are not required as concepts are related to memories and lnput and outputs         PO3       No design & development concepts included as the topics are related to memories and IO         PO4       Investigation are not included as it related to standard concepts of memories and IO         PO5       Tools are not required for these topics         PO6       Its not related to society usage         PO5       Tools are not used for environment and sustainability         PO8       No ethics are included in this topic         PO6       Its not relat		PO2	Applying concepts of calculating Bit reversed index generaion	_3
P04       Investigation are not included as it related to standard concepts of interfacing         P05       Tools are not required for these topics         P06       Its not related to society usage         P07       Architectures are not used for environment and sustainability         P08       No ethics are included in this topic         P09       No team work is required to know basics         P010       Communication and any documentation not required         P011       Project management and finance management are not needed         P012       Its not a life long learning process         C09       P01       Understanding the concepts of memory and parallel input outputs of memories         P02       Application are not required as concepts are related to memories and Input and outputs         P03       No design & development concepts included as the topics are related to memories and Input and outputs         P04       Investigation are not included as it related to standard concepts of memories and IO         P05       Tools are not required for these topics         P06       Its not related to society usage         P05       Tools are not required to know basics         P06       Its not related to society usage         P07       Architectures are not used for environment and sustainability         P08       No ethics are included in th		PO3	No design & development concepts included as the topics are	
of interfacing         PO5       Tools are not required for these topics         PO6       Its not related to society usage         PO7       Architectures are not used for environment and sustainability         PO8       No ethics are included in this topic         PO9       No team work is required to know basics         PO10       Communication and any documentation not required         PO11       Project management and finance management are not needed         PO12       Its not a life long learning process         CO9       PO1       Understanding the concepts of memory and parallel input outputs of memories         PO2       Application are not required as concepts are related to memories and Input and outputs         PO3       No design & development concepts included as the topics are related to memories and IO         PO5       Tools are not required for these topics         PO6       Its not related to society usage         PO6       Its not related to society usage         PO4       Investigation are not included as it related to standard concepts of memories and IO         PO5       Tools are not required for these topics         PO6       Its not related to society usage         PO6       No ethics are included in this topic         PO8       No ethics are included in this topic			related to interfacing concepts	
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PO8No ethics are included in this topicPO9No team work is required to know basicsPO10Communication and any documentation not requiredPO11Project management and finance management are not neededPO12Its not a life long learning processCO10PO1Understanding the concepts of SSI,CODEC,Speech processing,Image processingPO2Applying of knowledge is not required		PO6	Its not related to society usage	
PO9No team work is required to know basicsPO10Communication and any documentation not requiredPO11Project management and finance management are not neededPO12Its not a life long learning processCO10PO1Understanding the concepts of SSI,CODEC,Speech processing,Image processingPO2Applying of knowledge is not required		PO7	Architectures are not used for environment and sustainability	
PO10       Communication and any documentation not required         PO11       Project management and finance management are not needed         PO12       Its not a life long learning process         CO10       PO1         Understanding       the         processing,Image processing         PO2       Applying of knowledge is not required		PO8	No ethics are included in this topic	
PO11       Project management and finance management are not needed         PO12       Its not a life long learning process         CO10       PO1         Understanding       the concepts of SSI,CODEC,Speech processing,Image processing         PO2       Applying of knowledge is not required		PO9	No team work is required to know basics	
PO12       Its not a life long learning process         CO10       PO1         Understanding       the         concepts       of         SSI,CODEC,Speech         processing,Image processing         PO2       Applying of knowledge is not required		PO10	Communication and any documentation not required	
CO10       PO1       Understanding       the       concepts       of       SSI,CODEC,Speech         processing,Image       processing         PO2       Applying of knowledge is not required		PO11	Project management and finance management are not needed	
processing,Image processing       PO2     Applying of knowledge is not required		PO12	Its not a life long learning process	
PO2 Applying of knowledge is not required	CO10	PO1		
PO3 No design & development concepts included as the topics are				
		PO3	No design & development concepts included as the topics are	

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		related to application of DSP	
	PO4	Investigation are not included as it related to standard concepts	
		of DSP applicaitons	
	PO5	Tools are not required for these topics	
	PO6	Its not related to society usage	
	PO7	Architectures are not used for environment and sustainability	
	PO8	No ethics are included in this topic	
	PO9	No team work is required to know basics	
	PO10	Communication and any documentation not required	
	PO11	Project management and finance management are not needed	
	PO12	Its not a life long learning process	
L			

Note: Write justification for each CO-PO mapping.

### 5. Curricular Gap and Content

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					

Note: Write Gap topics from A.4 and add others also.

### 6. Content Beyond Syllabus

SNo	Gap Topic	Actions Planned	Schedule Planned	Resources Person	PO Mapping
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					

Note: Anything not covered above is included here.



# C. COURSE ASSESSMENT

### 1. Course Coverage

Mod	Title	Teaching		No. of	quest	tion in	Exam		CO	Levels
ule		Hours	CIA-	CIA-	CIA-	Asg	Extra	SEE		
#			1	2	3		Asg			
1	Introduction to Digital Signal	8	2	-	-	1		2	CO1,	L2
	Processing								CO2	
	Computational Accuracy in DSP									
	Implementations									
2	Architectures for Programmable	8	2	-	-	1		2	CO3	L2,L3
	Digital Signal - Processing									
	Devices:									
3	Programmable Digital Signal	8	-	2	-	1		2	CO4,	L3
	Processors								CO5	
4	Implementation of Basic DSP	8	-	2	-	1		2	CO6	L5
	Algorithms									
5	Interfacing Memory and Parallel	8	-	-	4	1		2	CO7,	L2
	I/O Peripherals to Programmable								C08	
	DSP Devices									
	Interfacing and Applications of									
	DSP Processors									
-	Total	40	4	4	4	5				

Note: Distinct assignment for each student. 1 Assignment per chapter per student. 1 seminar per test per student.

#### 2. Continuous Internal Assessment (CIA)

Evaluation	Weightage in Marks	CO	Levels
CIA Exam - 1	15	CO1, CO2, CO3, CO4	L2, I3,
CIA Exam - 2	15	CO5, CO6,	L3, L5
CIA Exam - 3	15	CO7, C08	L3
Assignment – 1	05	CO1, CO2, CO3, CO4	L2, I3,
Assignment – 2	05	CO5, CO6,	L3, L5
Assignment – 3	05	CO7, C08	L3
Seminar – 1		CO1, CO2, CO3, CO4	L2, I3,
Seminar – 2		CO5, CO6,	L3, L5
Seminar – 3		CO7, C08	L3

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Other Activities - define		2		CO1 to Co8	L2, L3, L5
– Slip test					

Final CIA Marks20-Note : Blooms Level in last column shall match with A.2 above.

D1. TEACHING PLAN – 1

### Module – 1

Title:	Introduction to Digital Signal Processing	Appr	8 Hrs
	Computational Accuracy in DSP Implementations	Time:	
а	Course Outcomes	-	Blooms
-	The student should be able to:	-	Level
1	Understand Basic concepts of DSP system	CO1	L2
2	Apply knowledge to evaluate errors for Implementation	CO2	L3
b	Course Schedule	_	_
Class No	Module Content Covered	CO	Level
1	Introduction	C01	L2
2	A Digital Signal Processing System The Sampling Process	C01	L2
3	Discrete Time Sequences	C01	L2
4	Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT)	C01	L2
5	Linear Time-Invariant Systems	C01	L2
6	Digital Filters	C01	L2
7	Decimation and Interpolation.	C01	L3
8	Number Formats for Signals and Coefficients in DSP Systems	C01	L2
9	Dynamic Range and Precision	C01	L2
10	Sources of Error in DSP Implementation.	C01	L2
С	Application Areas	СО	Level
1	Basics of DSP help in designing the algorithms	CO1	L2
2	During implementation process errors can be analyzed and minimized	CO2	L3
d	Review Questions		_
1	Explain with the help of mathematical equations how signed numbers can be multiplied. The sequence $x(n) = [3,2,-2,0,7]$ . It is interpolated using interpolation sequence $bk=[0.5,1,0.5]$ and the interpolation factor of 2. Find the interpolated sequence $y(m)$		L3
2	An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT X(k) determine the analog and digital frequency spacing between adjacent X(k0 elements. Also, determine analog and digital frequencies corresponding to $k=60$ .		L3

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3		gram explain the scheme of the DSP system.	CO1	L2				
4		What are the important issues to be considered in	CO1	L3				
		implementing a DSP system? Explain in detail.						
5		pling is required? Explain the sampling process.	CO1	L2				
6	block diagram	Define decimation and interpolation process. Explain them using CO1 L5 Nock diagrams and equations. With a neat diagram explain the cheme of a DSP system.						
7	With an examp process.	le explain the need for the low pass filter in decimation	CO1	L5				
8		ter $y(n) = (x(n)+x(n-1)+x(n-2))/3$ . Determine i) System gnitude and phase function iii) Step response iv) Group	CO1	L5				
9	List the major high speed pro	CO1	L2					
10	Explain how to	simulate the impulse responses of FIR and IIR filters.	CO1	L2				
11	-	o method of sampling rate conversions used in DSP suitable block diagrams and examples. Draw the spectrum.	CO1	L2				
12	-	namic range of a signal increases by6db for each Ised to represent its value	CO2	L3				
13	-	dynamic range and percentage resolution for a block format with a 4 bit exponent used in a 16 bit fixed r	CO2	L3				
14	that uses a. 16 point floa	dynamic range and percentage resolution of a signal ating point format floating point format with 24 bits for the mantissa and xponent	CO2	L3				
е	Experiences		_	_				
1								
2								
3								
4								
5								

# Module – 2

Title:	Architectures for Programmable Digital Signal - Processing Devices:	Appr	8 Hrs
		Time:	
а	Course Outcomes	-	Blooms
-	The student should be able to:	-	Level
1	Apply knowledge of DSP computational building blocks to achieve	CO2	L3

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pyright ©20	17. cAAS. All rights rese	rved. architecture or processor.				
	speed in DSF a					
b	Course Schedule		_	_		
	Module Cont	ent Covered	co	Leve		
No						
1	Introduction					
2	Basic Architect	tural Features				
3	DSP Computat	ional Building Blocks				
4	Bus Architectu	ire and Memory				
5	Data Addressi	ng Capabilities				
6	Address Gene	ration Unit				
7	Programmabil	ity and Program Execution Speed Issues				
8	Features for E	xternal Interfacing.				
С	Application A	CO	Level			
1	Understand D	SP processing	CO2	L2		
2	Programming	DSP processors	CO2	L5		
d	<b>Review Ques</b>	stions	-	-		
1	Explain imple	mentation of 8- tap FIR filter, (i) pipelined using MAC	CO2	L5		
	-	parallel using two MAC units. Draw block diagrams				
2		le of a shifter in DSP? Explain the implementation of 4-	CO2	L3		
	-	barrel shifter, with a diagram				
3	Identify the	CO2	L5			
	-	ructions & their operations				
		D #1234h iii) ADD 5678h iv) ADD +*addreg				
4		ematic diagram of the saturation logic and explain the	CO2	L3		
-	same.		603	12		
5	-	he circular addressing mode and bit reversal addressing	CO2	L2		
6		lemented in a DSP. Irpose of program sequencer.	CO2	L2		
7		ture of a 4X4 Braun multiplier, Explain its concept. What	C02	L2 L5		
/		is required to carry out multiplication of signed	02	LJ		
		nment on the speed of the multiplier				
8		bits in a MAC unit of DSP. Consider a MAC unit whose	CO2	L5		
0		-bit numbers. How many guard bits should be provided				
	-	cts have to be added in the accumulator to prevent				
	-	dition? What is the overall size of the accumulator				
	required?					
9	-	ock diagram explain ALU of DSP system	CO2	L3		

	required?		
9	With a neat block diagram explain ALU of DSP system	CO2	L3
10	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	CO2	L3
11	The 256 unsigned numbers, 16 bit each are to be summed up in a	CO2	L5
	processor. How many guard bits are needed to prevent overflow		
12	How will you implement an 8X8 multiplier using 4X4 multipliers as	CO2	L5

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	the building bl	ocks.				
е	Experiences		-	-		
1			CO1	L2		
2						

# E1. CIA EXAM - 1

### a. Model Question Paper - 1

Crs Code:		15EC751 Sem: VII Marks: 30 Time: 75									
Cour		DSP Algori	thms and A	rchitecture							
-	-	- Note: Answer any 3 questions, each carry equal marks. Mark					CO	Level			
1	a	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail.					<b>s</b> 7	CO1	L5		
	b		-				etermine i) Syst response iv) Gro		8	CO1	L5
2	a	system, w		le block d			sions used in I mples. Draw		7	CO1	L2
	b	can be mu using inte	ltiplied. Th rpolation	e sequence sequence b	x(n) = [3, 2]	2,-2,0,7 5] and	w signed numb '].It is interpola the interpolat	ted	8	CO1	L3
3	a	Compute t that uses a. 16 point b. 32 bit p	the dynami	c range an pint format g point forr	id percenta	ge resc	plution of a sig		8	CO2	L3
	b	With a nea	t block diag	gram explai	n ALU of DS	SP syste	m		7	CO2	L2
4	a	modificatio	on is requ	uired to c	• *	nultipli	n its concept. W cation of sign		8	CO2	L5
	b	Explain cir	cular buffe	r addressing	g mode ii) P	arallelis	sm iii) Guard bit	ts	7	CO2	L3

# b. Assignment -1

Note: A distinct assignment to be assigned to each student.

Model Assignment Questions							
Crs Code:	CS501PC	Sem:	I	Marks:	5 / 10	Time:	90 – 120 minutes
Course: Design and Analysis of Algorithms							
Note: Food student to ensure 2. 2 posice ments. Food posice ment comics and morely							

Note: Each student to answer 2-3 assignments. Each assignment carries equal mark.

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SNo	USN	Assignment Description	Mark s	CO	Level
1	1KT16EC401	Explain with the help of mathematical equations how signed numbers can be multiplied. The sequence $x(n) = [3,2,-2,0,7]$ . It is interpolated using interpolation sequence $bk=[0.5,1,0.5]$ and the interpolation factor of 2. Find the interpolated sequence $y(m)$		C01	L3
2	1KT15EC001	An analog signal is sampled at the rate of 8KHz. If 512 samples of this signal are used to compute DFT X(k) determine the analog and digital frequency spacing between adjacent X(k0 elements. Also, determine analog and digital frequencies corresponding to k=60.		CO1	L3
3	1KT15EC003	With a neat diagram explain the scheme of the DSP system.		CO1	L2
4	1KT16EC403	What is DSP? What are the important issues to be considered in designing and implementing a DSP system? Explain in detail.		CO1	L3
5	1KT15EC004	Why signal sampling is required? Explain the sampling process.	5	CO1	L2
6	1KT15EC005	Define decimation and interpolation process. Explain them using block diagrams and equations. With a neat diagram explain the scheme of a DSP system.		C01	L5
7	1KT15EC006	With an example explain the need for the low pass filter in decimation process.	5	CO1	L5
8	1KT15EC008	For the FIR filter $y(n)=(x(n)+x(n-1)+x(n-2))/3$ . Determine i) System Function ii) Magnitude and phase function iii) Step response iv) Group Delay		C01	L5
9	1KT15EC011	List the major architectural features used in DSP system to achieve high speed program execution.	5	CO1	L2
10	1KT16EC406	Explain how to simulate the impulse responses of FIR and IIR filters.	5	CO1	L2
11	1KT15EC012	Explain the two method of sampling rate conversions used in DSP system, with suitable block diagrams and examples. Draw the corresponding spectrum.	5	C01	L2
12	1KT15EC013	Show the dynamic range of a signal increases by6db for each additional bit used to represent its value	5	CO2	L3
13	1KT15EC015	Compute the dynamic range and percentage resolution for a block floating point format with a 4 bit exponent used in a 16 bit fixed point processor		CO2	L3
14	1KT15EC017	Compute the dynamic range and percentage resolution of a signal that uses	5	CO2	L3

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		a. 16 point floating point format			
		b. 32 bit point floating point format with 24 bits for the			
		mantissa and 8 bits for the exponent			
15	1KT15EC019	Explain implementation of 8- tap FIR filter, (i) pipelined	5	CO2	L5
		using MAC units and (ii) parallel using two MAC units.			
		Draw block diagrams			
16	1KT14EC068	What is the role of a shifter in DSP? Explain the	5	CO2	L3
		implementation of 4-bit shift right barrel shifter, with a	2		
		diagram			
17	1KT15EC020	Identify the addressing modes of the operands in each of	5	CO2	L5
		the following instructions & their operations	2	001	25
		i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg			
18	1KT15EC021	Draw the schematic diagram of the saturation logic and	5	CO2	L3
10		explain the same.	5	002	LJ
19	1KT16EC408	Explain how the circular addressing mode and bit reversal	5	CO2	L2
		addressing mode are implemented in a DSP.	5	002	22
20	1KT15EC022	Explain the purpose of program sequencer.	5	CO2	L2
21	1KT15EC023	Give the structure of a 4X4 Braun multiplier, Explain its	5	CO2	L5
21		concept. What modification is required to carry out	J	002	LJ
		multiplication of signed numbers? Comment on the speed			
		of the multiplier			
22	1KT15EC024		5	CO2	L5
22	1111020021	Explain guard bits in a MAC unit of DSP. Consider a MAC	2	02	LD
		unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added			
		in the accumulator to prevent overflow condition? What is			
		the overall size of the accumulator required?			
23	1KT15EC025		5	602	1.2
	1KT16EC411	With a neat block diagram explain ALU of DSP system	5	CO2	L3
24	INTIOLETII	Explain circular buffer addressing mode ii) Parallelism iii) Guard bits	С	CO2	L3
25	1KT15EC028	The 256 unsigned numbers, 16 bit each are to be summed	5	CO2	L5
		up in a processor. How many guard bits are needed to			
		prevent overflow			
26	1KT15EC029	How will you implement an 8X8 multiplier using 4X4	5	CO2	L5
		multipliers as the building blocks.			
27	1KT15EC030	Identify the addressing modes of the operands in each of	5	CO1	L3
		the following instructions & their operations			
		i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg			
28	1KT15EC031	Draw the schematic diagram of the saturation logic and	5	CO1	L3
		explain the same.			
29	1KT15EC032	Explain how the circular addressing mode and bit reversal	5	CO1	L2
		addressing mode are implemented in a DSP.			
30	1KT16EC412		5	CO1	L3
30	1KT16EC412	Explain the purpose of program sequencer.	5	CO1	L3

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Copyrigh 31		cAAS. All rig	Give conce multi	red. the structure of a 4X4 Braun multiplier, Explain its ept. What modification is required to carry out plication of signed numbers? Comment on the speed e multiplier	5	C01	L2
32		5EC037	unit v bits s in the	in guard bits in a MAC unit of DSP. Consider a MAC whose inputs are 24-bit numbers. How many guard should be provided if 512 products have to be added a accumulator to prevent overflow condition? What is verall size of the accumulator required?	5	CO1	L5
33	1KT1	5EC038	With a	a neat block diagram explain ALU of DSP system	5	CO1	L5
34	1KT1	5EC039	Expla Guaro	in circular buffer addressing mode ii) Parallelism iii) d bits	5	CO1	L5
35	1KT1	5EC041	up in	256 unsigned numbers, 16 bit each are to be summed a a processor. How many guard bits are needed to ent overflow	5	CO1	L2
36	1KT1	6EC416		will you implement an 8X8 multiplier using 4X4 pliers as the building blocks.	5	CO1	L2
37	1KT1	5EC043	using	in implementation of 8- tap FIR filter, (i) pipelined MAC units and (ii) parallel using two MAC units. block diagrams	5	CO1	L2
38	1KT1	5EC044		is the role of a shifter in DSP? Explain the ementation of 4-bit shift right barrel shifter, with a am	5	CO2	L3
39	1KT1	5EC045	the fo	ify the addressing modes of the operands in each of ollowing instructions & their operations O B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg	5	CO2	L3
40	1KT1	6EC419		the schematic diagram of the saturation logic and in the same.	5	CO2	L3
41	1KT1	5EC046	-	in how the circular addressing mode and bit reversal essing mode are implemented in a DSP.	5	CO2	L5
42	1KT1	5EC047	Expla	in the purpose of program sequencer.	5	CO2	L3
43	1KT1	5EC048	Give conce multi	the structure of a 4X4 Braun multiplier, Explain its ept. What modification is required to carry out plication of signed numbers? Comment on the speed e multiplier	5	CO2	L5
44		5EC049	unit v bits s in the the o	in guard bits in a MAC unit of DSP. Consider a MAC whose inputs are 24-bit numbers. How many guard should be provided if 512 products have to be added accumulator to prevent overflow condition? What is verall size of the accumulator required?	5	CO2	L3
45		5EC051		a neat block diagram explain ALU of DSP system	5	CO2	L2
46	IKTI	5EC052	Expla	in circular buffer addressing mode ii) Parallelism iii)	5	CO2	L2

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	1471650050	Guard bits			
47	1KT15EC053	The 256 unsigned numbers, 16 bit each are to be summed	5	CO2	L5
		up in a processor. How many guard bits are needed to			
	1271(50421	prevent overflow			
48	1KT16EC421	How will you implement an 8X8 multiplier using 4X4	5	CO2	L5
	11/11/1500055	multipliers as the building blocks.			
49	1KT15EC055	Explain implementation of 8- tap FIR filter, (i) pipelined	5	CO2	L3
		using MAC units and (ii) parallel using two MAC units.			
	11/11/10/06/	Draw block diagrams			
50	1KT15EC056	What is the role of a shifter in DSP? Explain the	5	CO2	L3
		implementation of 4-bit shift right barrel shifter, with a			
		diagram			
51	1KT15EC058	Identify the addressing modes of the operands in each of	5	CO2	L5
		the following instructions & their operations			
		i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg			
52	1KT15EC061	Draw the schematic diagram of the saturation logic and	5	CO2	L5
		explain the same.			
53	1KT16EC423	Explain how the circular addressing mode and bit reversal	5		
		addressing mode are implemented in a DSP.			
54	1KT16EC424	Explain the purpose of program sequencer.	5		
55	1KT15EC062	Give the structure of a 4X4 Braun multiplier, Explain its	5		
		concept. What modification is required to carry out			
		multiplication of signed numbers? Comment on the speed			
		of the multiplier			
56	1KT16EC426	Explain guard bits in a MAC unit of DSP. Consider a MAC	5		
		unit whose inputs are 24-bit numbers. How many guard			
		bits should be provided if 512 products have to be added			
		in the accumulator to prevent overflow condition? What is			
		the overall size of the accumulator required?			
57	1KT15EC067	With a neat block diagram explain ALU of DSP system	5		
58	1KT15EC007	Explain circular buffer addressing mode ii) Parallelism iii)	5		
		Guard bits			
59	1KT15EC010	The 256 unsigned numbers, 16 bit each are to be summed	5		
		up in a processor. How many guard bits are needed to			
		prevent overflow			
60	1KT15EC014	How will you implement an 8X8 multiplier using 4X4	5		
		multipliers as the building blocks.	-		
61	1KT15EC026	Explain implementation of 8- tap FIR filter, (i) pipelined	5		
		using MAC units and (ii) parallel using two MAC units.	J		
		Draw block diagrams			
62	1KT15EC054	What is the role of a shifter in DSP? Explain the	5		
02		-	C		
		implementation of 4-bit shift right barrel shifter, with a			

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		diagram		
63	1KT16EC422	Identify the addressing modes of the operands in each of	5	
		the following instructions & their operations		
		i)ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg		
64	1KT15EC059	Draw the schematic diagram of the saturation logic and	5	
		explain the same.		
65	1KT15EC063	Explain how the circular addressing mode and bit reversal	5	
		addressing mode are implemented in a DSP.		
66	1KT15EC064	Explain the purpose of program sequencer.	5	
67		Give the structure of a 4X4 Braun multiplier, Explain its	5	
		concept. What modification is required to carry out		
		multiplication of signed numbers? Comment on the speed		
		of the multiplier		

# D2. TEACHING PLAN – 2

# Module - 3

Title:	Programmable Digital Signal Processors	Appr	8 Hrs
		Time:	
а	Course Outcomes	-	Blooms
_	The student should be able to:	-	Level
1	Evaluate time and space complexity and calculate performance	CO5	L2
2	Understand searching and sorting schemes	CO6	L3
b	Course Schedule		
Class No	Module Content Covered	со	Level
1	Introduction, Commercial Digital Signal-processing Devices	CO3	L2
2	Data Addressing Modes of TMS32OC54XX	CO3	L3
3	Memory Space of TMS32OC54xx Processors	CO3	L2
4	Program Control.	CO3	L2
5	Detail Study of TMS320C54X & 54xx	CO4	L2
6	Instructions and Programming	CO4	L3
7	On - Chip Peripherals	CO4	L3
8	Interrupts of TMS32OC54XX Processors	CO4	L3
C	Application Areas	СО	Level
1	Programming TMS320C54xx processor using data addressing modes	CO3	L3
2	Understand instructions ,on chip peripherals and Interrupts	CO4	L3
d	Review Questions	_	
1	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	CO3	L2

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	. cAAS. All rights reserved. Write an explanatory note on direct addressing mode of	CO3	L3
-	TMS320C54XX processors. Give example.		
I	Describe the operation of the following instructions of TMS320C54XX processors. i) MPY *AR2-,*AR4+0B (ii) MAC *ar5+,#1234h,A (iii) STH A,1,*AR2 iv) SSBX SXM		L2
	With a block diagram explain the indirect addressing mode of TMS320C54XX processor using dual data memory operand.	CO3	L3
	What is the function of an address generation unit explain with the help of block diagram.	CO3	L2
	Why circular buffers are required in DSP processor? How they are implemented?	CO3	L5
	Explain the direct addressing mode of the TMS320C54XX processor with the help of a block diagram.	CO3	L2
	Describe the multiplier/adder unit of TMS320c54xx processor with a neat block diagram.	CO3	L3
9	Describe any four data addressing modes of TMS320c54xx processor	CO3	L3
•	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.		L2
11	Explain PMST register.	CO3	L2
12	Explain the functioning of barrel shifter in TMS320C54XX processor	CO3	L2
13	Explain sequential and other types of program control	CO3	L2
	With an example each, explain immediate, absolute, and direct addressing mode.	CO3	L3
16	Explain the functioning of barrel shifter in TMS320C54XX processor.	CO3	L2
17	Explain sequential and other types of program control	CO3	L2
•	Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.		L5
19	Explain PMST register.	CO3	L2
	Compare architectural features of TMS320C25 and DSP6000 fixed point digital signal processors.	CO3	L2
21	Describe Host Port Interface and explain its signals.	CO4	L2
1	writes an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation $y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2)$ with usual notations. Find y (n) for signed 16 bit data samples and 16 bit constants.		L5
	Describe the pipelining operation of TMS320C54XX processors.	CO4	L3
24	Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals.	CO4	L2
	Expalin the differents types of interrupts in TMS320C54xx Processors.	CO4	L2
	Describe the operation of the following instructions of TMS 320c54xx		L3

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opyright ©20	processor, with example Describe the operation of hardware timer		
	with neat diagram		
27		604	1.4
27	By means of a figure explain the pipeline operation of the following	CO4	L4
	sequence of instruction if the initial values of AR1,AR3,A are		
	104,101,2 and the values stored in the memory locations		
	101,102,103,104 are 4,6,8,12. Also provide the values of registers		
~ ~	AR3, AR1,T & A.		
28	Describe the operation of the following instructions of TMS320C54XX	CO4	L4
	processors.		
29	Describe the operation of the following instructions of TMS320C54XX	CO4	L4
	processors.		
30	Explain the following assembler directives of TMS320C54XX	CO4	L4
	processors (i) .mmregs (ii) .global (iii) .include 'xx' (iv) .data ( v) .end		
	(vi) .bss		
31	Describe Host Port Interface and explain its signals.	CO4	L4
32	writes an assembly language program of TMS320C54XX processors	CO4	L5
	to compute the sum of three product terms given by the equation		
	y(n)=h(0)x(n)+h(1)x(n-1)+h(2)x(n-2) with usual notations. Find y (n)		
	for signed 16 bit data samples and 16 bit constants.		
33	Describe the pipelining operation of TMS320C54XX processors.	CO4	L2
34	Explain the operation of serial I/O ports and hardware timer of	CO4	L3
	TMS320C54XX on chip peripherals.		
35	Expalin the differents types of interrupts in TMS320C54xx Processors.	CO4	L2
е	Experiences	_	-
1		CO1	L2
2			
3			
4		CO3	L3
5			

# Module – 4

Class No	Module Content Covered	CO	Level
b	Course Schedule		
2	Able to implement the 8 point Butterfly diagram	CO6	L5
1	Understand the Q notation and Different Filters	CO5	L2
-	The student should be able to:	-	Level
а	Course Outcomes	-	Blooms
		Time:	
Title:		Appr	16 Hrs

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	7. cAAS. All rights reser	<sup>ved.</sup> The Q – notation	CO5	L3
	FIR Filters		CO5	L5
	IIR Filters		CO5	L5
		and Decimation Filters (one example in each case).	CO5	L5
	-	An FFT Algorithm for DFT Computation	CO6	L2
	Overflow and	-	C06	L2
	Bit – Reversed	-	CO6	L2
		Implementation on the TMS32OC54xx.	CO6	 L5
	Application /		CO	Level
	IIR and FIR Filt		C05	L3
		scaling technique	CO6	L5
-	Review Ques	-	_	_
1	Describe the	e importance of Q-notation in DSP algorithm	CO5	L1
	implementatio	on with examples. What are the values represented by		
	16– bit fixed	point number N=4000h in Q15, Q10, Q7 notations?		
	Explain how	the FIR filter algorithms can be implemented using		
	TMS320c54xx	processor.		
2	Explain with t	he help of a block diagram and mathematical equations	CO5	L3
	the implemen			
	required.			
		mbly language program for TMS320C54XX processor to	CO5	L2
	implement an			
		rawback of using linear interpolation for implementing		L4
		ter in TMS320C54XX processor? Show the memory		
		or the filter implementation.	COF	12
	Briefly explain		CO5	L2
		e value of each of the following 16- bit numbers	CO5	L5
	-	sing the given Q-notations: Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as	C05	L2
		(iv) – 0.3125 as a Q15 number.	05	LZ
		mbly language program for TMS320C54XX processors	CO5	L3
		o Q15 numbers to produce Q15 number result.	205	LJ
		erpolation filter? Explain the implementation of digital	CO5	L4
		using FIR filter and poly phase sub filter.		
	-	e value of each of the following 16- bit numbers	CO5	L1
		sing the given Q-notations:		
	-	Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as	CO5	L4
		r (iv) -0.3125 as a Q15 number.		
		mbly language program for TMS320C54XX processors	CO5	L3
		o Q15 numbers to produce Q15 number result.		
13	Briefly explain	IIR filters.	CO2	L2
14	Describe the	e importance of Q-notation in DSP algorithm	CO5	L3

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	implementation with examples. What are the values represented by		
	16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?		
15	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	CO5	L2
16	Explain with the help of a block diagram and mathematical equations	CO5	L3
	the implementation of a second order IIR filter. No program code is required.		
17	Write the assembly language program for TMS320C54XX processor to	CO5	L4
	implement an FIR filter.		<b>L</b> ·
18	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	CO5	L4
19	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	CO5	L5
20	Derive the equation to implement a butterfly structure In DITFFT algorithm.	CO6	L2
21	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	CO6	L3
22	Why zero padding is done before computing the DFT?	CO6	L2
23	What do you mean by bit-reversed index generation and how it is	CO6	L3
	implemented in TMS320C54XX DSp assembly language?		
24	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	CO6	L3
25	Explain a general DITFFT butterfly in place computation structure.	CO6	L2
26	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT.	CO6	L3
27	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation.	CO6	L2
28	Determine the following for a 128-point FFT computation: (i) number of stages (ii) number of butterflies in each stage (iii) number of butterflies needed for the entire computation (iv) number of butterflies that need no twiddle factors (v) number of butterflies that require real twiddle factors (vi) number of butterflies that require complex twiddle factors.	CO6	L5
29	Explain, how scaling prevents overflow conditions in the butterfly computation.	CO6	L2
30	Explain, how scaling prevents overflow conditions in the butterfly computation.	CO6	L2
31	With the help of the implementation structure, explain the FFT	CO6	L3

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	-	DIT-FFT computation on TMS320C54XX processors.		
		ale factor for all butterflies.		
	Derive the ec algorithm.	quation to implement a butterfly structure In DITFFT	CO6	L5
	-	dd/subtract and multiply operations are needed to outterfly structure?	CO6	L5
	Write the subi same.	routine for bit reversed address generation. Explain the	CO6	L3
35	Why zero pade	ding is done before computing the DFT?	CO6	L3
	-	mean by bit-reversed index generation and how it is in TMS320C54XX DSp assembly language?	CO6	L3
		utine program to find the spectrum of the transformed S320C54XX DSP.	CO6	L3
	algorithm for	p of the implementation structure, explain the FFT DIT-FFT computation on TMS320C54XX processors. ale factor for all butterflies	CO6	L3
	of stages (ii) butterflies ne butterflies tha	e following for a 128-point FFT computation: (i) number number of butterflies in each stage (iii) number of eeded for the entire computation (iv) number of at need no twiddle factors (v) number of butterflies that widdle factors (vi) number of butterflies that require dle factors	CO6	L2
е	Experiences		-	_
1				
2				
3				
4				
				l

# E2. CIA EXAM - 2

5

# a. Model Question Paper - 2

Crs		15EC751 Sem: VII Marks: 30 Time: 75 minutes									
Code	e:										
Coui	rse:	DSP Algori	DSP Algorithms and Architecture								
-	-	Note: Ans	swer any	2 questi	ons, each c	arry equ	al mark	s.	Mark	CO	Level
									S		
1		implement 16– bit fix	ation with ked point ow the Fl	n example number IR filter a	of Q-nota es. What are N=4000h in Ilgorithms ca	the valu Q15, Q	es repres 10, Q7 n	ented by	<b>/</b> ?	CO5	LI

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	b	Explain with th	e help of a block diagram and mathematical equations	7	CO5	L3
		the implement required.	ation of a second order IIR filter. No program code is			
2		Write the asser implement an I	nbly language program for TMS320C54XX processor to FIR filter.	8	CO5	L4
			importance of Q-notation in DSP algorithm n with examples. What are the values represented by oint number N=4000h in Q15, Q10, Q7 notations?	7	CO5	L3
3		Explain, how s computation.	scaling prevents overflow conditions in the butterfly	7	CO6	L2
			mean by bit-reversed index generation and how it is n TMS320C54XX DSp assembly language?	8	CO6	L3
4			erpolation filter? Explain the implementation of digital sing FIR filter and poly phase sub filter.	7	CO5	L5
	b	Explain a gene	ral DITFFT butterfly in place computation structure.	8	CO6	L2

# b. Assignment – 2

Note: A distinct assignment to be assigned to each student.

				Model A	Assignment	Questions				
Crs C	ode:	CS501F	C Sem:	1	Marks:	5 / 10	Time:	90 - 120	) minu	tes
Cours	se:	Design	and Analysis	of Algorith	ims					
Note:	Each	student	to answer 2	-3 assignm	ents. Each	assignmen	t carries equ	al mark.		
SNo	l	JSN		Assign	ment Des	cription		Mark	СО	Leve
								S		
1	1KT	16EC401	Describe the	e importan	ce of Q-no	tation in I	DSP algorith	m 5	CO5	L1
			implementat	ion with	examples.	What ar	e the value	es		
			represented	by 16- bi	t fixed poi	nt numbe	r N=4000h	in		
			Q15, Q10,	Q7 notat	ions? Expla	ain how	the FIR filt	er		
			algorithms	can be i	mplemente	d using	TMS320c54>	٢X		
			processor.							
2	1KT	15EC001	Explain with	the help of	f a block di	agram and	mathematic	al 5	CO5	L3
			equations th	ie impleme	ntation of a	a second c	order IIR filte	er.		
			No program	code is req	juired.					
3	1KT	15EC003	Write the as	sembly lar	nguage pro	gram for <sup>-</sup>	TMS320C54>	x	C05	L2
			processor to	implement	t an FIR filte	er.				
4	1KT	16EC403	What is the	drawback	of using	linear int	erpolation f	or 5	CO5	L4
			implementin	g of an FIF	R filter in T	MS320C54	XX processo	r?		
			Show the	memory	organiza	tion for	the filt	er		
			implementat	ion.						
5	1KT	15EC004	Briefly expla	in IIR filters	5			5	CO5	L2
6	1KT	15EC005	Determine t	he value	of each of	the follo	wing 16– k	oit 5	CO5	L5
			numbers re	presented	using the	given Q-	-notations:	(i)		

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		0.3125 as a Q15 number (ii) - 0.3125 as a Q15 number.			
7	1KT15EC006	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:(i) 4400h as a Q10 number (ii) 4400h as a Q7 number	5	CO5	L2
8	1KT15EC008	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
9	1KT15EC011	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L4
10	1KT16EC406	Determine the value of each of the following 16- bit numbers represented using the given Q-notations:	5	CO5	L1
11	1KT15EC012	(i) 4400h as a Q10 number (ii) 4400h as a Q7 number (iii) 0.3125 as a Q15 number (iv) -0.3125 as a Q15 number.	5	CO5	L4
12	1KT15EC013	Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.	5	CO5	L3
13	1KT15EC015	Briefly explain IIR filters.	5	CO5	L2
14	1KT15EC017	Describe the importance of Q-notation in DSP algorithm implementation with examples. What are the values represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?	5	CO5	L3
15	1KT15EC019	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L2
16	1KT14EC068	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
17	1KT15EC020	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	5	CO5	L4
18	1KT15EC021	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	CO5	L4
19	1KT16EC408	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L5
20	1KT15EC022	Derive the equation to implement a butterfly structure In DITFFT algorithm.	5	CO6	L2
21	1KT15EC023	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	5	CO6	L3
22	1KT15EC024	Why zero padding is done before computing the DFT?	5	CO6	L2

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Copyright 23	Copyright ©2017. cAAS. All rig 23 1KT15EC025			do you mean by bit-reversed index generation and	5	CO6	L3
25	IXII	520025		it is implemented in TMS320C54XX DSp assembly	2	00	LS
			langu				
24	1KT1	6EC411	-	a subroutine program to find the spectrum of the	5	CO6	L3
				formed data using TMS320C54XX DSP.	-		
25	1KT1	5EC028	Expla	in a general DITFFT butterfly in place computation	5	CO6	L2
			struc	ture.			
26	1KT1	5EC029	Deter	rmine the number of stages and number of butterflies	5	CO6	L3
			in ea	ch stage and the total number of butterflies needed			
			for th	ne entire computation of 512 point FFT.			
27	1KT1	5EC030	-	in how the bit reversed index generation can be done	5	CO6	L2
				pt FFT. Also write a TMS320C54xx program for 8 pt			
	11/1	5EC031	-	FFT bit reversed index generation.		606	
28	1	JECUJI		rmine the following for a 128-point FFT computation: mber of stages (ii) number of butterflies in each stage	5	CO6	L5
				number of butterflies needed for the entire			
			l` ´	putation (iv) number of butterflies that need no			
			-	lle factors (v) number of butterflies that require real			
				lle factors (vi) number of butterflies that require			
				blex twiddle factors.			
29	1KT1	5EC032	Expla	in, how scaling prevents overflow conditions in the	5	CO6	L2
			butte	rfly computation.			
30	1KT1	6EC412	Expla	in, how scaling prevents overflow conditions in the	5	CO6	L2
				rfly computation.			
31	1KT1	5EC036		the help of the implementation structure, explain the	5	CO6	L3
				algorithm for DIT-FFT computation on TMS320C54XX			
22	11/1	5EC037	-	essors. Use $\frac{1}{4}$ as a scale factor for all butterflies.	-	<u> </u>	
32	1	JEC037		e the equation to implement a butterfly structure In -T algorithm.	5	CO6	L5
33	1KT1	5EC038		many add/subtract and multiply operations are	5	CO6	L5
				ed to compute the butterfly structure?	J		LJ
34	1KT1	5EC039	-	the subroutine for bit reversed address generation.	5	CO6	L3
				in the same.	-		
35	1KT1	5EC041	-	zero padding is done before computing the DFT?	5	CO6	L3
36	1KT1	6EC416	What	do you mean by bit-reversed index generation and	5	CO6	L3
			how	it is implemented in TMS320C54XX DSp assembly			
			langu	lage?			
37	1KT1	5EC043		a subroutine program to find the spectrum of the	5	CO6	L3
			-	formed data using TMS320C54XX DSP.			
38	1KT1	5EC044		the help of the implementation structure, explain the	5	CO6	L3
				algorithm for DIT-FFT computation on TMS320C54XX			
			proce	essors. Use ¼ as a scale factor for all butterflies			

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39	IKII	5EC045	(i) nu (iii) comp twidc twidc	rmine the following for a 128-point FFT computation: mber of stages (ii) number of butterflies in each stage number of butterflies needed for the entire putation (iv) number of butterflies that need no dle factors (v) number of butterflies that require real dle factors (vi) number of butterflies that require plex twiddle factors	5	CO6	L2
40	1KT1	6EC419	imple repre Q15, algor	ribe the importance of Q-notation in DSP algorithm ementation with examples. What are the values esented by 16- bit fixed point number N=4000h in Q10, Q7 notations? Explain how the FIR filter ithms can be implemented using TMS320c54xx essor.	5	CO5	L1
41	1KT1	5EC046	equa	in with the help of a block diagram and mathematical tions the implementation of a second order IIR filter. rogram code is required.	5	CO5	L3
42		5EC047		the assembly language program for TMS320C54XX essor to implement an FIR filter.	5	CO5	L2
43	1KT1	5EC048	imple Show	is the drawback of using linear interpolation for ementing of an FIR filter in TMS320C54XX processor? the memory organization for the filter ementation.	5	CO5	L4
44	1KT1	5EC049	Briefl	y explain IIR filters	5	CO5	L2
45	1KT1	5EC051		rmine the value of each of the following 16- bit pers represented using the given Q-notations:	5	CO5	L5
46	1KT1	5EC052		00h as a Q10 number (ii) 4400h as a Q7 number (iii) 25 as a Q15 number (iv) - 0.3125 as a Q15 number.	5	CO5	L2
47		5EC053	proce	an assembly language program for TMS320C54XX essors to multiply two Q15 numbers to produce Q15 per result.	5	CO5	L3
48	1KT1	6EC421		is an interpolation filter? Explain the implementation gital interpolation using FIR filter and poly phase sub	5	CO5	L4
49	1KT1	5EC055		rmine the value of each of the following 16- bit pers represented using the given Q-notations:	5	CO5	L1
50	1KT1	5EC056		00h as a Q10 number (ii) 4400h as a Q7 number (iii) 25 as a Q15 number (iv) -0.3125 as a Q15 number.	5	CO5	L4
51		5EC058	proce	an assembly language program for TMS320C54XX essors to multiply two Q15 numbers to produce Q15 per result.	5	CO5	L3
52		5EC061	Briefl	y explain IIR filters.	5	CO2	L2
53	1KT1	6EC423	Desc	ribe the importance of Q-notation in DSP algorithm	5	CO5	L3

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Copyright	ıt ©2017. cAAS. All rig	implementation with examples. What are the values			
		represented by 16- bit fixed point number N=4000h in Q15, Q10, Q7 notations?			
54	1KT16EC424	Explain how the FIR filter algorithms can be implemented using TMS320c54xx processor.	5	CO5	L2
55	1KT15EC062	Explain with the help of a block diagram and mathematical equations the implementation of a second order IIR filter. No program code is required.	5	CO5	L3
56	1KT16EC426	Write the assembly language program for TMS320C54XX processor to implement an FIR filter.	5	CO5	L4
57	1KT15EC067	What is the drawback of using linear interpolation for implementing of an FIR filter in TMS320C54XX processor? Show the memory organization for the filter implementation.	5	C05	L4
58	1KT15EC007	What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase sub filter.	5	CO5	L5
59	1KT15EC010	Derive the equation to implement a butterfly structure In DITFFT algorithm.	5	CO6	L2
60	1KT15EC014	How may add/subtract and multiply operations are needed to compute the butterfly structure? Write the subroutine for bit reversed address generation. Explain the same.	5	CO6	L3
61	1KT15EC026	Why zero padding is done before computing the DFT?	5	CO6	L2
62	1KT15EC054	What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L3
63	1KT16EC422	Write a subroutine program to find the spectrum of the transformed data using TMS320C54XX DSP.	5	CO6	L3
64	1KT15EC059	Explain a general DITFFT butterfly in place computation structure.	5	CO6	L2
65	1KT15EC063	Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT.	5	CO6	L3
66	1KT15EC064	Explain how the bit reversed index generation can be done in 8 pt FFT. Also write a TMS320C54xx program for 8 pt DIT-FFT bit reversed index generation.	5	CO6	L2
67		What do you mean by bit-reversed index generation and how it is implemented in TMS320C54XX DSp assembly language?	5	CO6	L5

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D3. TEACHING PLAN - 3

### Module – 5

Title:	Divide and Conquer	Appr Time:	18Hrs
а	Course Outcomes	_	Blooms
_	The student should be able to:	_	Level
1	Understand memories,Bus interfaces,DMA	C07	L2
2	Understand DSP Interfacing applications	C08	L3
b	Course Schedule		-
Class No	Module Content Covered	CO	Level
1	Introduction, Memory Space Organization	C07	L2
2	External Bus Interfacing Signals.	C07	L3
3	Memory Interface, Parallel I/O Interface	C07	L3
4	Programmed I/O,Interrupts and I/O Direct Memory Access	C07	L5
5	Introduction, Synchronous Serial Interface	C08	L2
6	A CODEC Interface Circuit, DSP Based Bio-telemetry Receiver	C08	
7	A Speech Processing System	C08	L3
8	An Image Processing System.	C08	L3
С	Application Areas	CO	Level
1	Memory interfacing with DSP processor	C07	L3
2	Interrupts and Parallel I/O Interrupts	CO8	L4
d	Review Questions	-	-
1	Explain an interface between an A/D converter and the TMS320C54XX	C07	L1
	processor in the programmed I/O mode.		
2	Describe DMA with respect to TMS320C54XX processors	C07	L3
3	Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.	C07	L2
4	Explain the memory interface block diagram for the TMS 320 C54xx processor.	C07	L3
5	Draw the I/O interface timing diagram for read - write read sequence of operation.	CO8	L2
6	What are interrupts? How interrupts are handled by C54xx DSP Processors.	CO8	L4
7	Explain the memory interface block diagram for the TMS 320 C54xx processor.	CO8	L3
8	Draw the I/O interface timing diagram for read - write read sequence of operation.	CO8	L3
9	What are interrupts? How interrupts are handled by C54xx DSP Processors.	CO8	L3

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	17. cAAS. All rights reser		_	
	-	memory system with address range 000800h - 000fffh	CO8	L5
	-	ocessor using 2kx8 SRAM memory chips.		
	5	memory system with address range 000800h - 000fffh	CO8	L4
	for a c5416 pro	ocessor using 2kx8 SRAM memory chips.		
12	Explain an inte	rface between an A/D converter and the TMS320C54XX	CO8	L3
	processor in th	e programmed I/O mode.		
13	Describe DMA \	with respect to TMS320C54XX processors.	CO8	L2
14	Draw the timir	ng diagram for memory interface for read-read-write	CO8	L3
	sequence of op	eration. Explain the purpose of each signal involved.		
15	Explain the me	mory interface block diagram for the TMS 320 C54 $xx$	CO8	L3
	processor.			
16	Draw the I/O ir	nterface timing diagram for read – write read sequence	CO8	L5
	of operation			
17	What are inte	rrupts? How interrupts are handled by C54xx DSP	CO8	L3
	Processors.			
18	What are interr	upts? What are the classes of interrupts available in the	CO8	L3
	TMS320C54xx	processor.		
19	With the help c	of a block diagram, explain the image compression and	CO8	L4
	reconstruction			
20	Write a pseud	o algorithm heart rate(HR), using the digital signal	CO8	L3
	processor.			
21	Explain briefly	the building blocks of a PCM3002 CODEC device. What	CO8	L3
	do you underst	and by a DSP based biotelemetry receiver?		
22	With the help o	f block diagram explain JPEG algorithm.	CO8	L3
23	Explain with the	e neat diagram the operation of pitch detector.	CO8	L3
24	Explain with a	neat diagram, the synchronous serial interface between	CO8	L3
	the C54xx an	d a CODEC device. Explain the operation of pulse		
	position modul			
25	Explain with a	neat block diagram the operation, the operation of the	CO8	L3
	pitch detector.			
26	Explain PCM30	02 CODEC, with the help of neat block diagram.	CO8	L3
27	Explain DSP ba	ased biotelemetry receiver system, with the help of a	CO8	L3
	block schemati	c diagram.		
28	Explain the me	mory interface block diagram for the TMS 320 C54xx	CO8	L3
	processor.	-		
29	Draw the I/O ir	nterface timing diagram for read - write read sequence	CO8	L3
	of operation			
		upts? What are the classes of interrupts available in the	CO8	L3
	TMS320C54xx			
	Experiences		_	_
1	-			
2				
_	L			



# E3. CIA EXAM - 3

# a. Model Question Paper - 3

Crs		15EC751	Sem:	VII	Marks:	30	Time:	75	5 minut	es	
Code	e:										
Coui	rse:	DSP Algori	thms and a	Architecture							
-	-	Note: Ans	Note: Answer any 2 questions, each carry equal marks.								Level
1	а	Explain the processor.	-	interface bl	ock diagra	m for tl	ne TMS 320	C54xx	7	C07	L3
	b		_	-			or read-read n signal invol		8	C07	L2
2	a	· ·	an interfa 4XX proce	ace betwee ssor in the p		,	nverter and 10de.	d the	2 7	C07	L1
	b	Describe D	MA with r	espect to TM	1S320C54>	(X proce	ssors			C07	L3
3	a	Draw the I		ce timing dia	agram for	read - w	rite read sec	luence	8	CO8	L5
	b	Describe D	MA with r	espect to TM	1S320C54>	(X proce	ssors.		7	CO8	L2
4	а	Explain PC	M3002 CC	DEC, with t	ne help of	neat blo	ck diagram.		8	CO8	L3
	b	Explain DS block sche		-	receiver s	system,	with the hel	p of a	1 7	CO8	L3

### b. Assignment – 3

Note: A distinct assignment to be assigned to each student.

				Mod	el Assignmen	t Quest	ions			
Crs C	ode:	CS501P	C Sem:	VII	Marks:	5	Time:	90 - 120	90 - 120 minutes	
Cours	se:	Design	and Analysis	of Algo	rithms					
Note:	Each	student	to answer 2-	-3 assig	nments. Each	assign	ment carries equa	al mark.		
SNo	ι	JSN		Ass	ignment Des	criptio	on	Mark	CO	Level
								S		
1	1KT	16EC401	Explain an i	nterface	e between an	A/D d	converter and th	e 5	C07	L1
	TMS320C54XX processor in the programmed I/O mode				med I/O mode.					
2	1KT	15EC001	Describe DM	A with r	espect to TMS	320C5	4XX processors	5	C07	L3
3	1KT	15EC003	Draw the tin	ning dia	gram for me	mory ir	nterface for read	- 5	C07	L2
			read-write s	equence	e of operatior	. Expla	in the purpose o	of		
			each signal i	nvolved						
4	1KT	16EC403	Explain the	memory	interface blo	ock dia	gram for the TM	S 5	C07	L3
		320 C54xx processor.								
5	1KT	15EC004	Draw the I/O	interfa	ce timing diag	ram fo	r read – write rea	d 5	CO8	L2
			sequence of	operatio	on.					

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		cAAS. All rig 5EC005	1			CO8	1.4
6				are interrupts? How interrupts are handled by C54xx Processors.	5	08	L4
7	1KT1	5EC006	-	in the memory interface block diagram for the TMS C54xx processor.	5	CO8	L3
8	1KT1	5EC008	Draw	the I/O interface timing diagram for read - write read	5	CO8	L3
			seque	ence of operation.			
9	1KT1	5EC011		are interrupts? How interrupts are handled by C54xx Processors.	5	CO8	L3
10	1KT1	6EC406	0008	gn a data memory system with address range 00h - 000fffh for a c5416 processor using 2kx8 1 memory chips.	5	CO8	L5
11	1KT1	5EC012	0008	gn a data memory system with address range 00h - 000fffh for a c5416 processor using 2kx8 1 memory chips.	5	CO8	L4
12	1KT1	5EC013	-	in an interface between an A/D converter and the 20C54XX processor in the programmed I/O mode.	5	CO8	L3
13	1KT1	5EC015	Descr	ribe DMA with respect to TMS320C54XX processors.	5	CO8	L2
14	1KT1	5EC017	read-	the timing diagram for memory interface for read- write sequence of operation. Explain the purpose of signal involved.	5	CO8	L3
15	1KT1	5EC019	Expla	in the memory interface block diagram for the TMS C54xx processor.	5	CO8	L3
16	1KT1	4EC068	Draw	the I/O interface timing diagram for read - write read ence of operation	5	CO8	L5
17	1KT1	5EC020	What	are interrupts? How interrupts are handled by C54xx	5	CO8	L3
10	11/1	5EC021		Processors.		600	
18	1111	SEC021		are interrupts? What are the classes of interrupts able in the TMS320C54xx processor.	5	CO8	L3
19	1KT1	6EC408		the help of a block diagram, explain the image pression and reconstruction using JPEG encoder and der.	5	CO8	L4
20	1KT1	5EC022		a pseudo algorithm heart rate(HR), using the digital I processor.	5	CO8	L3
21		5EC023	Expla devic	in briefly the building blocks of a PCM3002 CODEC e. What do you understand by a DSP based lemetry receiver?	5	CO8	L3
22	1KT1	5EC024	With	the help of block diagram explain JPEG algorithm.	5	CO8	L3
23	1KT1	5EC025	Expla detec	in with the neat diagram the operation of pitch stor.	5	CO8	L3
24	1KT1	6EC411	Expla interf	in with a neat diagram, the synchronous serial face between the C54xx and a CODEC device. Explain operation of pulse position modulation (PPM) to	5	CO8	L3

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opyrigh	nt ©2017. cAAS. All rig				
		encode two biomedical signals.			
25	1KT15EC028	Explain with a neat block diagram the operation, the operation of the pitch detector.	5	CO8	L3
26	1KT15EC029	Explain PCM3002 CODEC, with the help of neat block diagram.	5	CO8	L3
27	1KT15EC030	Explain DSP based biotelemetry receiver system, with the help of a block schematic diagram.	5	CO8	L3
28	1KT15EC031	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
29	1KT15EC032	Draw the I/O interface timing diagram for read - write read sequence of operation	5	CO8	L3
30	1KT16EC412	What are interrupts? What are the classes of interrupts available in the TMS320C54xx processor.	5	CO8	L3
31	1KT15EC036	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	C07	L1
32	1KT15EC037	Describe DMA with respect to TMS320C54XX processors	5	C07	L3
33	1KT15EC038	Draw the timing diagram for memory interface for read- read-write sequence of operation. Explain the purpose of each signal involved.	5	C07	L2
34	1KT15EC039	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	C07	L3
35	1KT15EC041	Draw the I/O interface timing diagram for read - write read sequence of operation.	5	CO8	L2
36	1KT16EC416	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L4
37	1KT15EC043	Explain the memory interface block diagram for the TMS 320 C54xx processor.	5	CO8	L3
38	1KT15EC044	Draw the I/O interface timing diagram for read - write read sequence of operation.	5	CO8	L3
39	1KT15EC045	What are interrupts? How interrupts are handled by C54xx DSP Processors.	5	CO8	L3
40	1KT16EC419	Design a data memory system with address range 000800h - 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L5
41	1KT15EC046	Design a data memory system with address range 000800h - 000fffh for a c5416 processor using 2kx8 SRAM memory chips.	5	CO8	L4
42	1KT15EC047	Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.	5	CO8	L3
43	1KT15EC048	Describe DMA with respect to TMS320C54XX processors.	5	CO8	L2
44	1KT15EC049	Draw the timing diagram for memory interface for read- read-write sequence of operation. Explain the purpose of	5	CO8	L3

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each signal involved.

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1KT15EC051 Explain the memory interface block diagram for the TMS 45 5 CO8 L3 320 C54xx processor. 1KT15EC052 Draw the I/O interface timing diagram for read - write read CO8 L5 46 5 sequence of operation 1KT15EC053 47 What are interrupts? How interrupts are handled by C54xx 5 CO8 L3 DSP Processors. 1KT16EC421 48 What are interrupts? What are the classes of interrupts CO8 L3 5 available in the TMS320C54xx processor. 1KT15EC055 49 With the help of a block diagram, explain the image L4 5 CO8 compression and reconstruction using JPEG encoder and decoder. 1KT15EC056 50 Write a pseudo algorithm heart rate(HR), using the digital 5 CO8 L3 signal processor. 1KT15EC058 51 Explain briefly the building blocks of a PCM3002 CODEC CO8 L3 5 device. What do you understand by a DSP based biotelemetry receiver? 1KT15EC061 52 With the help of block diagram explain JPEG algorithm. 5 CO8 L3 1KT16EC423 53 Explain with the neat diagram the operation of pitch CO8 L3 5 detector. 1KT16EC424 Explain with a neat diagram, the synchronous serial 54 5 CO8 13 interface between the C54xx and a CODEC device. Explain the operation of pulse position modulation (PPM) to encode two biomedical signals. <sup>1KT15EC062</sup> Explain with a neat block diagram the operation, the 55 5 CO8 L3 operation of the pitch detector. 1KT16EC426 Explain PCM3002 CODEC, with the help of neat block 56 5 CO8 L3 diagram. 1KT15EC067 Explain DSP based biotelemetry receiver system, with the 57 5 CO8 L3 help of a block schematic diagram. 1KT15EC007 58 Explain the memory interface block diagram for the TMS 5 CO8 L3 320 C54xx processor. 1KT15EC010 59 Draw the I/O interface timing diagram for read - write read CO8 L3 5 sequence of operation 1KT15EC014 60 What are interrupts? What are the classes of interrupts CO8 13 5 available in the TMS320C54xx processor. 1KT15EC026 Explain an interface between an A/D converter and the 5 C07 L1 61 TMS320C54XX processor in the programmed I/O mode. 1KT15EC054 62 Describe DMA with respect to TMS320C54XX processors CO7 L3 5 1KT16EC422 L2 63 Draw the timing diagram for memory interface for read-5 CO7 read-write sequence of operation. Explain the purpose of

each signal involved.

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64	1KT1	5EC059	Expla	in the memory interface block diagram for the TMS	5	C07	L3
			320 0	C54xx processor.			
65	1KT1	5EC063	Draw	the I/O interface timing diagram for read - write read	5	CO8	L2
			seque	ence of operation.			
66	1KT1	5EC064	What	are interrupts? How interrupts are handled by C54xx	5	CO8	L4
			DSP F	Processors.			
67	Explain the memory interface block diagram for the TMS		5	CO8	L3		
			320 0	C54xx processor.			

# F. EXAM PREPARATION

# 1. University Model Question Paper

Cou	irse:	DSP Algorith	ms and Arch	nitecure			Month	/ Year	May /	2018
Crs	Code:	:: CS501PC Sem: I Marks: 100 Time:			180					
								1	minut	
-	Note	Answer all Fl	VE full ques	tions. All	questions carry	equal ma	rks.	Mark	CO	Leve
1				امني مام م			Duary the	S	<u> </u>	
1		with a neat c wave forms	nagram exp	fiain the	scheme of the D	SP system	. Draw the	08	CO1	L3
				71 14 14				07	<u> </u>	
					interpolated us				CO1	L3
				with in	terpolation factor	or 2. Dete	ermine the			
		interpolated	sequence.		OR					
		<b>F</b>	<b>(</b>					07	602	
_		Explain number formats for signals and co efficients in DSP systems Explain dynamic range and Precession						07	CO2	L2
	b	Explain dyna	mic range a	nd Prece	ssion			08	CO2	L2
2					SP works? Expla			07	CO3	L2
	b	Explain : i) ci	rcular addre	-	ode ii) parallelisr	n iii) Guar	d bits	09	CO3	L3
					OR					
-	a	Explain the bit reversed addressing mode for a 16 point FFT with a						08	CO3	L2
					neration of bina	-				
	b	With a neat b	olock diagra	m, explai	in the working o	f MAC unit	t.	07	CO3	L3
3		Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP					06	CO4	L3	
					nodes of TMS3	20C54XX	with one	10	CO4	L5
		example eac								
_	a	-		modes o	f the source op	erand in e	ach of the	10	CO5	L5
		-	-		*AR2+0B, A (ii)					
		ADD *AR2+%					, , ,			
					bler directives	of TMS	320C54XX	06	CO5	L5
		processors.	5							_
		•	ii) • global	iii) • incl	ude'xx' iv) • dat	a v) • end	vi) • bss			

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4	a	Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a QO number ii) 4400h as a Q7 number · 3125 as a Q15 number iv) 3125 as a Q15 number.	06	CO6	L5
	b	Write an ALP for the FIR filter with 200 input samples using 16 length circular buffers for the TMS320 DSP	10	CO6	L5
		OR			
-	a	Write a pseudo code to determine 8 point DFT using DIT FFT algorithm invoking butterfly subroutine in a nested loop for each stage	08	CO6	L3
	b	Write an ALP to multiply two Q15 numbers to produce a Q15 result for the TMS320 DSP	07	CO5	L3
5	a	Explain the working of DMA with respect to the TMS320 DSP processor.	08	C07	L2
	b	Explain the working of interrupts in TMS320 DSP	07	C07	L2
		OR			
	a	Explain the biotelemetry receiver system with the help of a block diagram.	07	CO8	L3
	b	With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.	08	CO8	L3

### 2. SEE Important Questions

Course:		Design and Ar	nalysis of Alg	gorithms			Month	/ Year	May /	2018
Crs Code:		CS501PC Sem: 3 Marks: 100 Time:				180				
							minut	es		
	Note	Answer all FIVE full questions. All questions carry equal marks.				-	-			
Mo dul	Qno.	mportant Question					Mark s	CO	Year	
e										
1	1	Nith a neat diagram explain the scheme of the DSP system.					06	CO1	2018	
	2	Mention the difference between FIR and IIR filters. Find the				06	CO1	2018		
		magnitude and phase response of an FIR filter represented by the								
		difference equation, $y(n) = 0.5x(n) - 0.5x(n - 1)$								
	3	Let $x[n] = [3, 2, -2, 0, 7]$ . It is interpolated using an interpolation					06	CO1	2017	
		filter bk = $[0.5, 1, 0.5]$ with interpolation factor 2. Determine the								
		interpolated sequence.								
	4	An analog sig	ınal is samp	led at the ra	ate of 8KHz	. If 512 sam	ples of	06	CO1	2017
		this signal are used to compute DFT x(k), determine analog and								
		digital freque	ency spacing	g between	adjacent x(	k) elements	. Also,			

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	determine analog and digital frequencies corresponding to K=64			
5	Explain number formats for signals and co efficients in DSP systems	08	C02	New
1	How does the barrel shifter in a DSP works? Explain with an example.	06	CO3	2018
2	Explain : i) circular addressing mode ii) parallelism iii) Guard bits	09	CO3	2017
3	With a neat block diagram, explain the working of MAC unit	08	CO3	2017
4	Explain the bit reversed addressing mode for a 16 point FFT with a neat diagram and step by step generation of binary code.	08	CO3	2018
5	With a neat block diagram, explain the working of MAC unit.	06	CO3	2015
1	Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP	06	CO4	2018
2	Explain any five addressing modes of TMS320C54XX with one example each.	10	CO4	2017
3	Explain the addressing modes of TMS320C54XX processor. Give examples.	10	CO4	2018
4	Identify the addressing modes of the source operand in each of the following instructions: (i) ADD, *AR2+0B, A (ii) ADD *AR2+, A (iii) ADD *AR2+%, A (iv) 3a DD #23h, A	10	CO5	2018
5	<ul> <li>Explain the following assembler directives of TMS320C54XX processors.</li> <li>i) • mmregs ii) • global iii) • include'xx' iv) • data v) • end vi) • bss</li> </ul>	06	CO5	2016
1	Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a QO number ii) 4400h as a Q7 number $\cdot$ 3125 as a Q15 number iv) 3125 as a Q15 number.	06	CO6	2017
2	Write an ALP for the FIR filter with 200 input samples using 16 length circular buffers for the TMS320 DSP	10	CO6	2018
3	explain scaling operation in DSP processor and derive the expression for optimal scaling factor for DIT FFT butterfly algorithm.	08	CO6	2018
4	Write a pseudo code to determine 8 point DFT using DIT FFT algorithm invoking butterfly subroutine in a nested loop for each stage	12	CO6	2017
5	Write an ALP to multiply two Q15 numbers to produce a Q15 result for the TMS320 DSP	06	CO5	2017
1	Explain the working of DMA with respect to the TMS320 DSP processor.	08	C07	2018
2	Explain the working of interrupts in TMS320 DSP	06	C07	2018
3	With a neat schematic diagram, design a data memory system with address range 000800h — 000FFFH for a C5416 processor. Use	08	C07	2017
	5 1 2 3 4 5 1 2 3 4 4 5 7 1 1 2 3 4 1 2 3 4 1 2 3 4 1 2	determine analog and digital frequencies corresponding to K=64         5       Explain number formats for signals and co efficients in DSP systems         1       How does the barrel shifter in a DSP works? Explain with an example.         2       Explain : i) circular addressing mode ii) parallelism iii) Guard bits         3       With a neat block diagram, explain the working of MAC unit         4       Explain the bit reversed addressing mode for a 16 point FFT with a neat diagram and step by step generation of binary code.         5       With a neat block diagram, explain the working of MAC unit.         1       Compare architectural features of TMS320C25, DSP56000 and ADSP2100 fixed point DSP         2       Explain the addressing modes of TMS320C54XX with one example each.         3       Explain the addressing modes of TMS320C54XX processor. Give examples.         4       Identify the addressing modes of TMS320C54XX processor. Give examples.         5       Explain the following assembler directives of TMS320C54XX processors.         i) ADD *AR2+%, A (iv) 3a DD #23h, A       5         5       Explain the following assembler directives of TMS320C54XX processors.         1       Determine the value of each of the following 16-bit numbers represented using the given Q-notations: i) 4400h as a Q0 number ii) 4400h as a Q7 number ·3125 as a Q15 number iv) 3125 as a Q15 number.         2       Write an ALP for the FIR filter with 200 input samples using 16 length c	determine analog and digital frequencies corresponding to K=64         5       Explain number formats for signals and co efficients in DSP systems       08         1       How does the barrel shifter in a DSP works? Explain with an example.       06         2       Explain : i) circular addressing mode ii) parallelism iii) Guard bits       09         3       With a neat block diagram, explain the working of MAC unit       08         4       Explain the bit reversed addressing mode for a 16 point FFT with a neat block diagram, explain the working of MAC unit.       06         5       With a neat block diagram, explain the working of MAC unit.       06         1       Compare architectural features of TMS320C25, DSP56000 and 06       06         ADSP2100 fixed point DSP       06         2       Explain any five addressing modes of TMS320C54XX processor. Give 10       10         example each.       10         4       Identify the addressing modes of TMS320C54XX processor. Give 10       10         examples.       10       AR2+%, A (iv) 3a DD #23h, A       10         5       Explain the following assembler directives of TMS320C54XX 06       06         processors.       i) · mmregs ii) · global iii) · include'xx' iv) · data v) · end vi) · bss       06         1       Determine the value of each of the following 16-bit numbers represented using the given Q-no	determine analog and digital frequencies corresponding to K=64       C02         5       Explain number formats for signals and co efficients in DSP systems       08       C02         1       How does the barrel shifter in a DSP works? Explain with an example.       06       C03         2       Explain : i) circular addressing mode ii) parallelism iii) Guard bits       09       C03         3       With a neat block diagram, explain the working of MAC unit       08       C03         4       Explain the bit reversed addressing mode for a 16 point FFT with a ost coast addressing mode for a 16 point FFT with a ost coast and the parameter of MAS 20025, DSP56000 and for aDSP 200 fixed point DSP       06       C03         2       Explain any five addressing modes of TMS320C54XX with one 10       C04       coast addressing modes of TMS320C54XX processor. Give 10       C04         3       Explain the addressing modes of TMS320C54XX processor. Give 10       C04       coast addressing modes of TMS320C54XX processor. Give 10       C04         4       Identify the addressing modes of the source operand in each of the 10       C05       cost addressing modes of TMS320C54XX processor.       06       C05         processors.       i)       ADD *AR2+%, A (iv) 3a DD #23h, A       06       C05       cost addressing notes of the following 16-bit numbers of represented using the given Q-notations: i) 4400h as a QO number ii) 4400h as a Q7 number 3125 as a Q15 number iv) 31

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		2Kx8 SRAM memory chips.							
	4	Explain the b	viotelemetry receiver system with the help of a block	06	CO8	2018			
		diagram.							
	5	With the help	of a block diagram, explain the image compression and	08	CO8	2017			
		reconstructio	econstruction using JPEG encoder and decoder.						